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DRX_ANT

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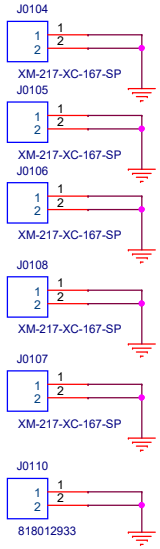
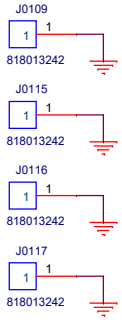
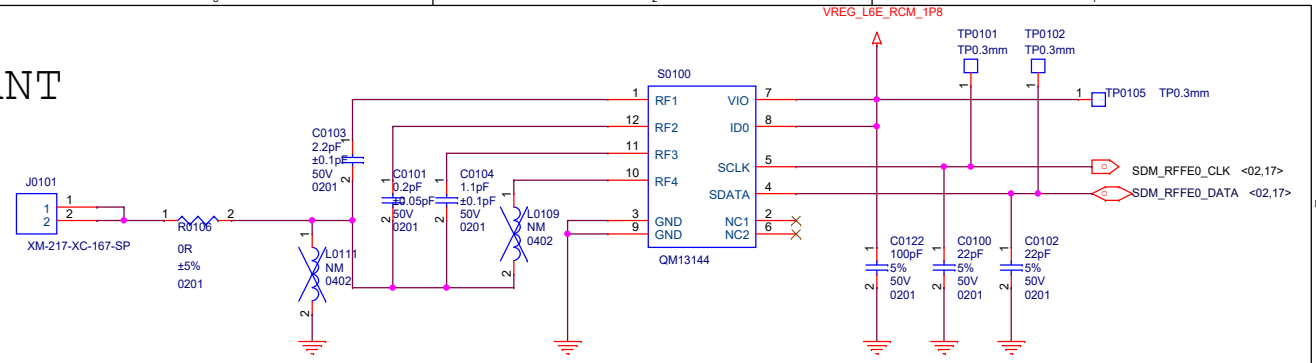
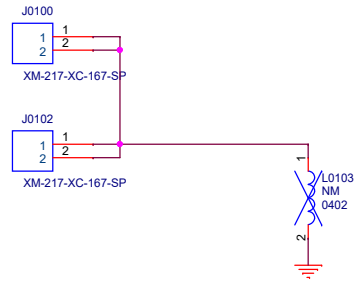
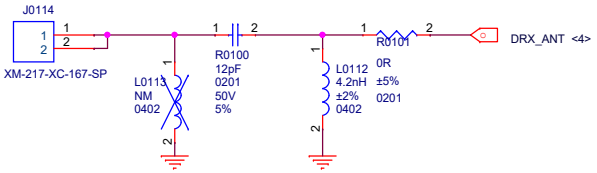


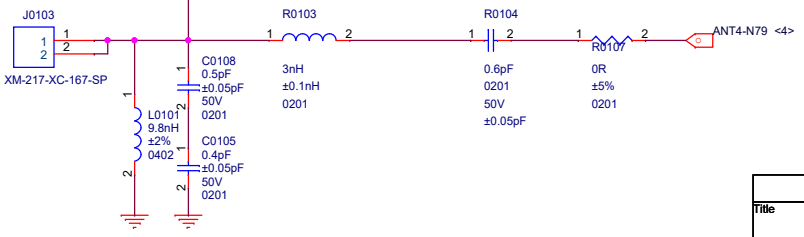








ANT4 n41 TRX+n78+n79 TRX



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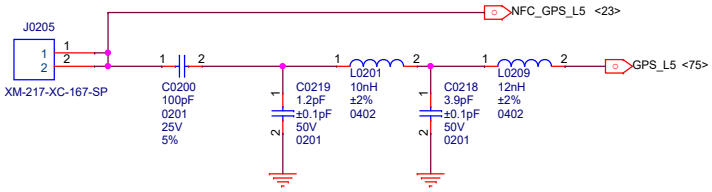
GPS L1+ WIFI2.4G CH0+WIFI 5G ANT2

GPS L5



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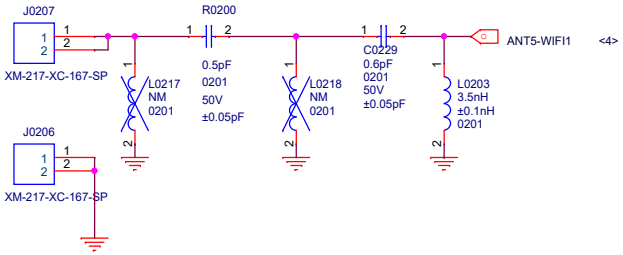
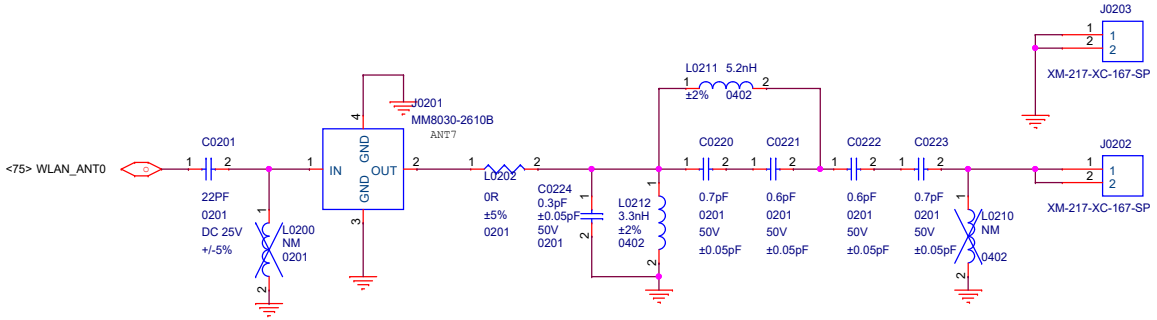
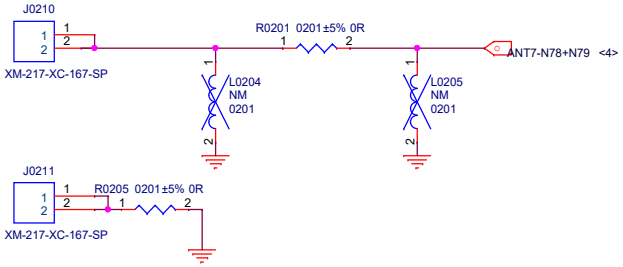




ANT7 N78+N79



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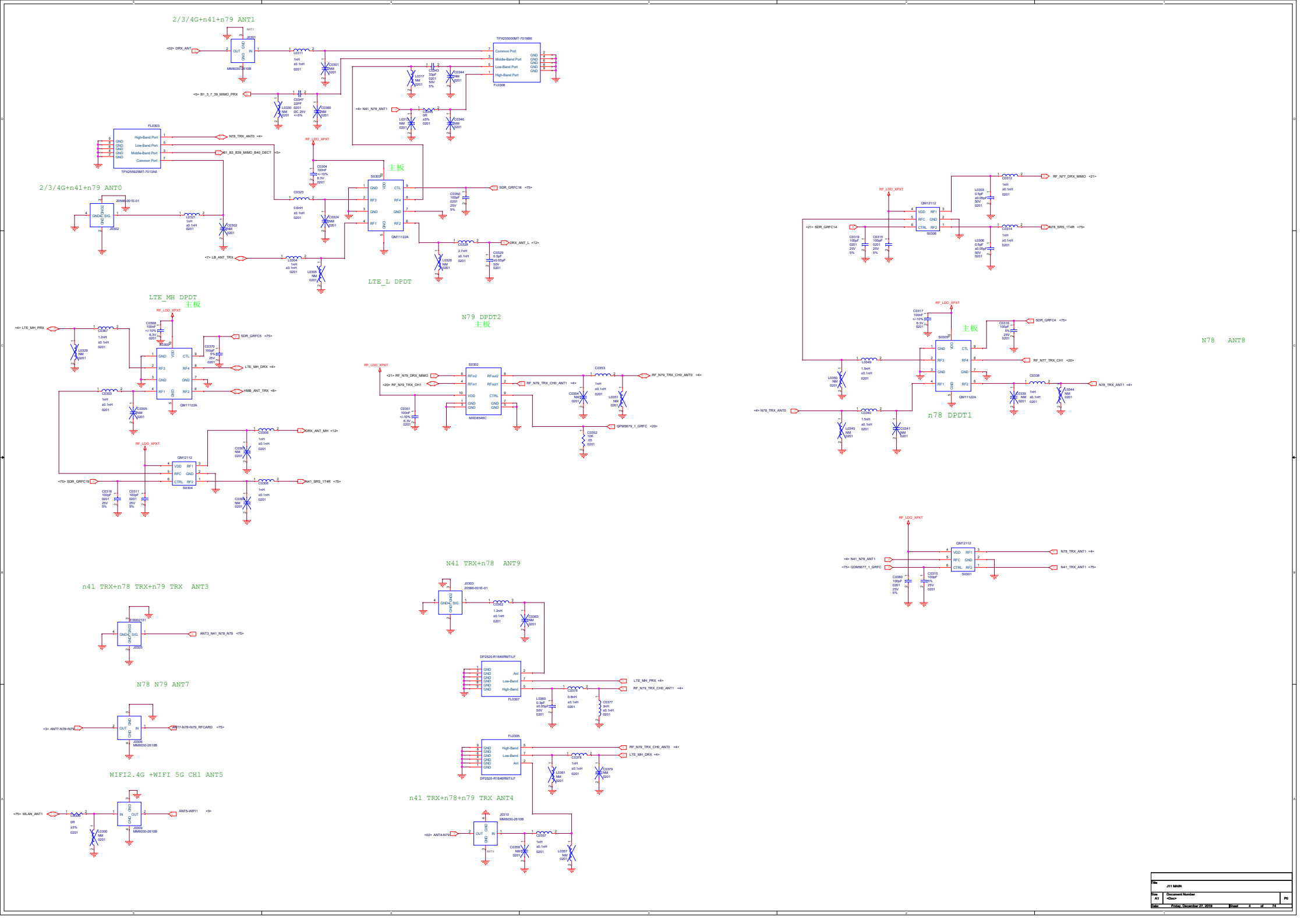
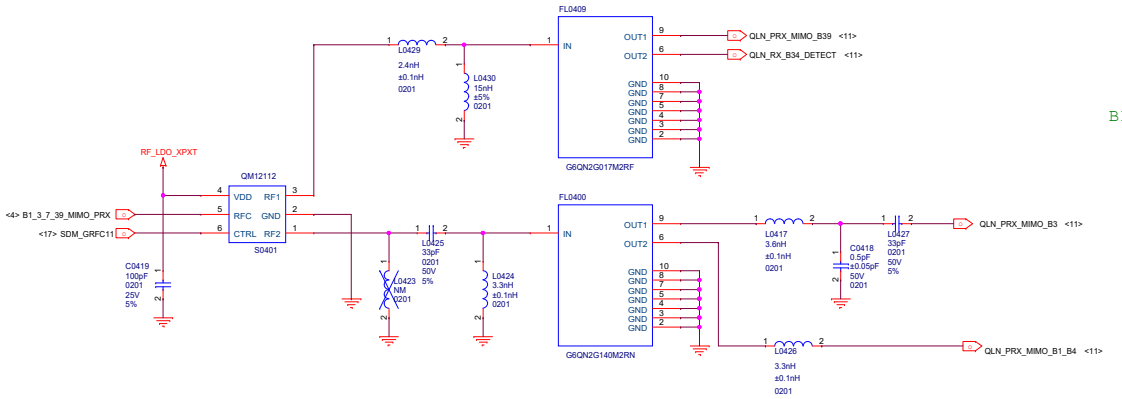

2/3/4G+n41+n79 ANT1
2/3/4G+n41+n79 ANT0
主板
LTE_L DPDT
LTE_MH DPDT
主板
N79 DPDT2
主板
n78 DPDT1
N78 ANT8
n41 TRX+n78 TRX+n79 TRX ANT3
N78 N79 ANT7
WIFI2.4G +WIFI 5G CH1 ANT5
N41 TRX+n78 ANT9
n41 TRX+n78+n79 TRX ANT4
J1 MAIN
Friday, December 27, 2019

B1+3+7+39 MIMO PRX



B1+3+7+39 MIMO DRX

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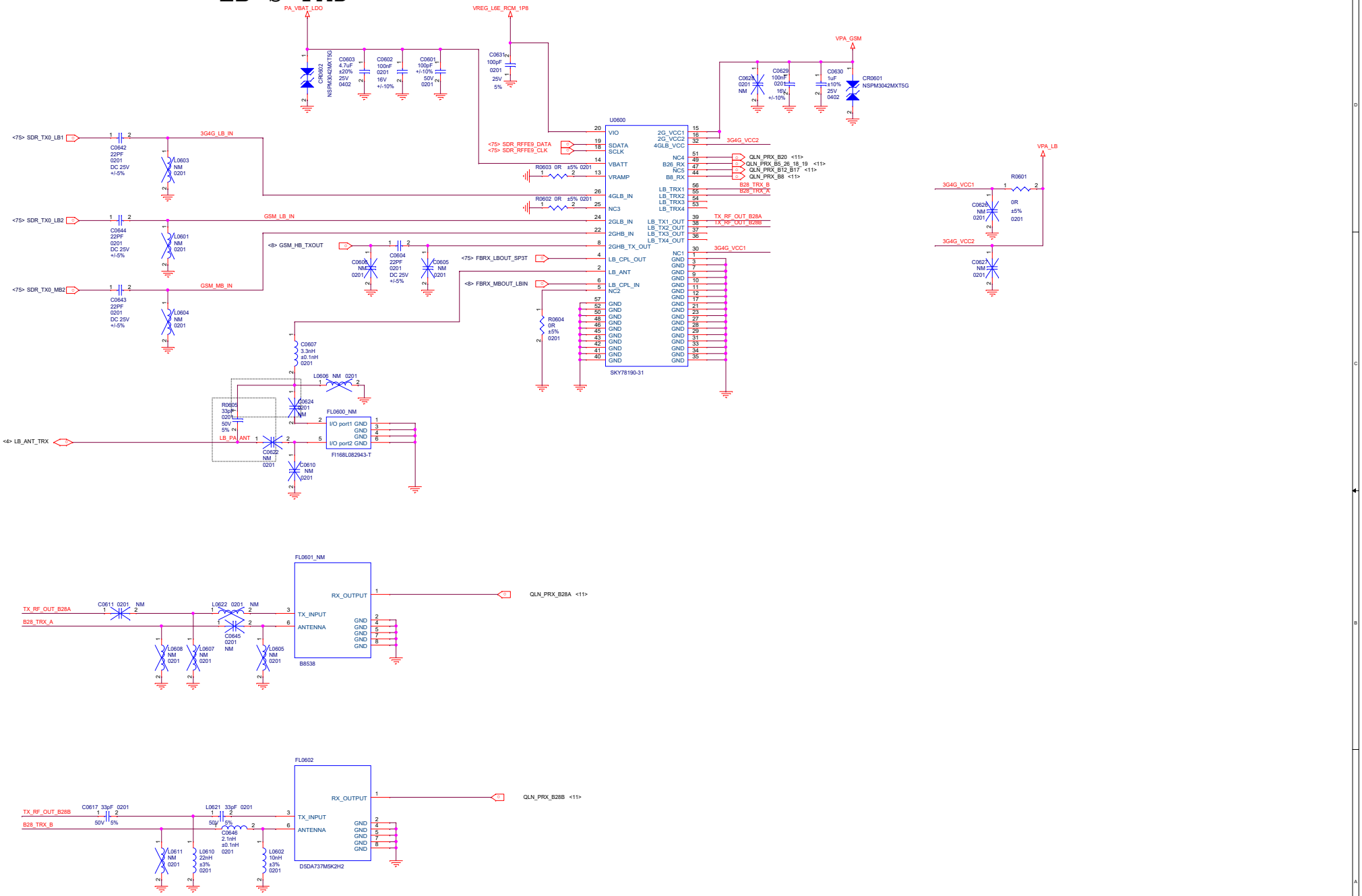
LB S-PAD



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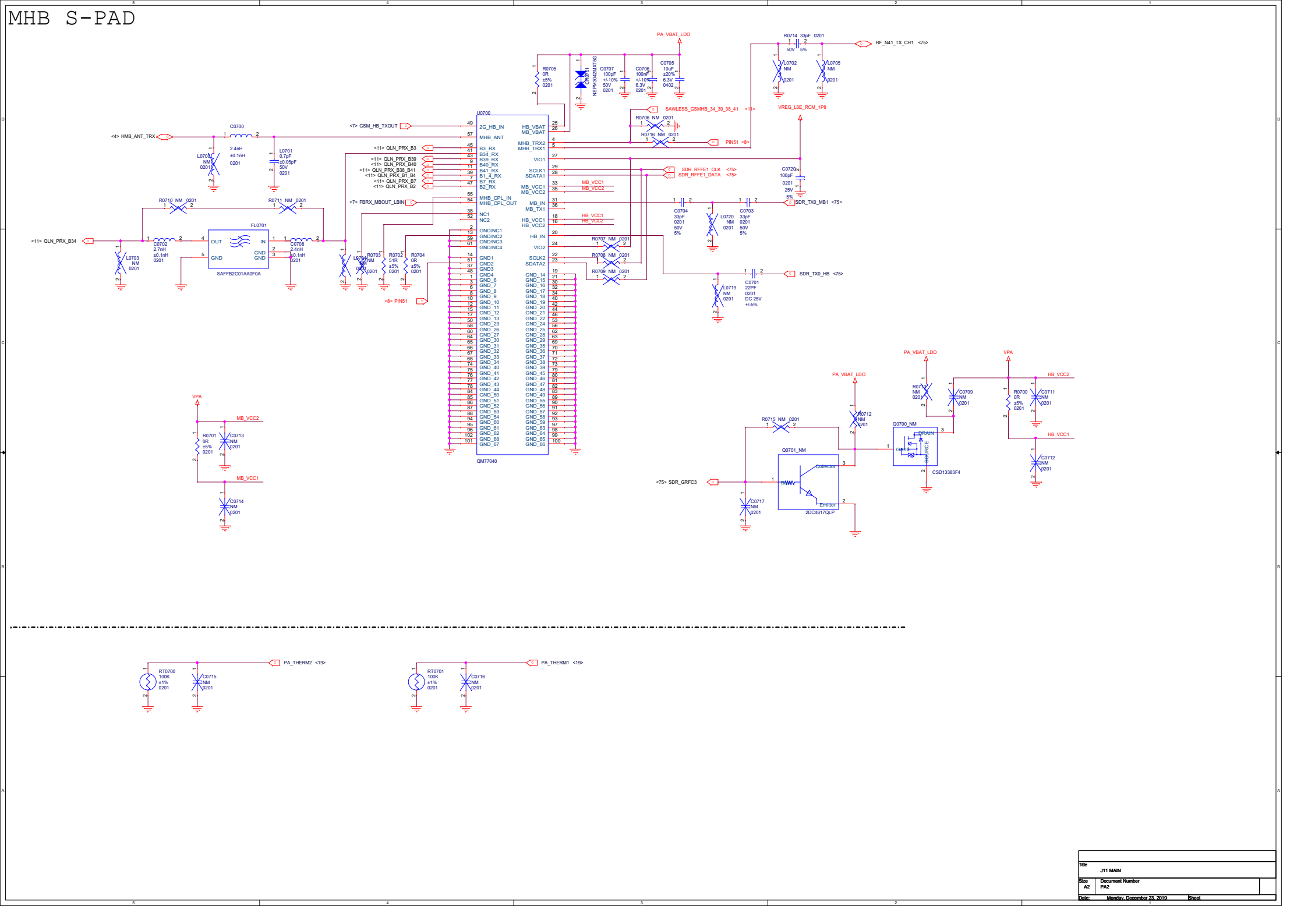
MHB S-PAD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R0705 0R ±5% 0201
D0700 NSPM830GM1T5G
C0707 100pF +/-10% 50V 0201
C0706 100nF +/-10% 6.3V 0201
C0705 10uF ±20% 6.3V 0402
R0714 33pF 0201 50V 5%
RF_N41_TX_CH1 <75>
L0702 NM 0201
L0705 NM 0201
SAWLESS_GSMHB_34_39_38_41 <13>
VREG_L6E_RCM_1P8
R0706 NM 0201
R0716 NM 0201
PIN51 <8>
U0700
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<4> HMB_ANT_TRX
C0700
L0700 NM 0201
2.4nH ±0.1nH 0201
L0701 0.7pF ±0.05pF 50V 0201
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<11> QLN_PRX_B39
<11> QLN_PRX_B40
<11> QLN_PRX_B38_B41
<11> QLN_PRX_B1_B4
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<11> QLN_PRX_B2
2G_HB_IN
MHB_ANT
B3_RX
B34_RX
B39_RX
B40_RX
B41_RX
B1_4_RX
B7_RX
B2_RX
MHB_CPL_IN
MHB_CPL_OUT
NC1
NC2
GND/NC1
GND/NC2
GND/NC3
GND/NC4
GND1
GND2
GND3
GND4
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_23
GND_26
GND_27
GND_30
GND_31
GND_32
GND_33
GND_34
GND_40
GND_41
GND_42
GND_43
GND_44
GND_50
GND_51
GND_52
GND_53
GND_54
GND_60
GND_61
GND_62
GND_68
GND_67
HB_VBAT
MB_VBAT
MHB_TRX2
MHB_TRX1
VIO1
SCLK1
SDATA1
MB_VCC1
MB_VCC2
MB_IN
MB_TX1
HB_VCC1
HB_VCC2
HB_IN
VIO2
SCLK2
SDATA2
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_24
GND_25
GND_28
GND_29
GND_35
GND_36
GND_37
GND_38
GND_39
GND_45
GND_46
GND_47
GND_48
GND_49
GND_55
GND_56
GND_57
GND_58
GND_59
GND_63
GND_64
GND_65
GND_66
QM77040
SDR_RFFE1_CLK <75>
SDR_RFFE1_DATA <75>
C0720 100pF 0201 25V 5%
SDR_TX0_MB1 <75>
C0704 33pF 0201 50V 5%
L0720 NM 0201
C0703 33pF 0201 50V 5%
R0707 NM 0201
R0708 NM 0201
R0709 NM 0201
L0719 NM 0201
C0701 22PF 0201 DC 25V +/-5%
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FL0701
SAFFB2G01AA0F0A
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R0711 NM 0201
C0702 2.7nH ±0.1nH 0201
L0703 NM 0201
C0708 2.4nH ±0.1nH 0201
L0704 NM 0201
R0703 0R ±5% 0201
R0702 51R ±5% 0201
R0704 0R ±5% 0201
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R0701 0R ±5% 0201
C0713 NM 0201
MB_VCC1
C0714 NM 0201
PA_VBAT_LDO
R0715 NM 0201
R0712 NM 0201
Q0701_NM
Collector
Base
Emitter
2DC4617QLP
<75> SDR_GRFC3
C0717 NM 0201
Q0700_NM
DRAIN
GATE
SOURCE
CSD13383F4
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C0709 NM 0201
VPA
HB_VCC2
R0700 0R ±5% 0201
C0711 NM 0201
HB_VCC1
C0712 NM 0201
RT0700 100K ±1% 0201
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Title
J11 MAIN
Size
A2
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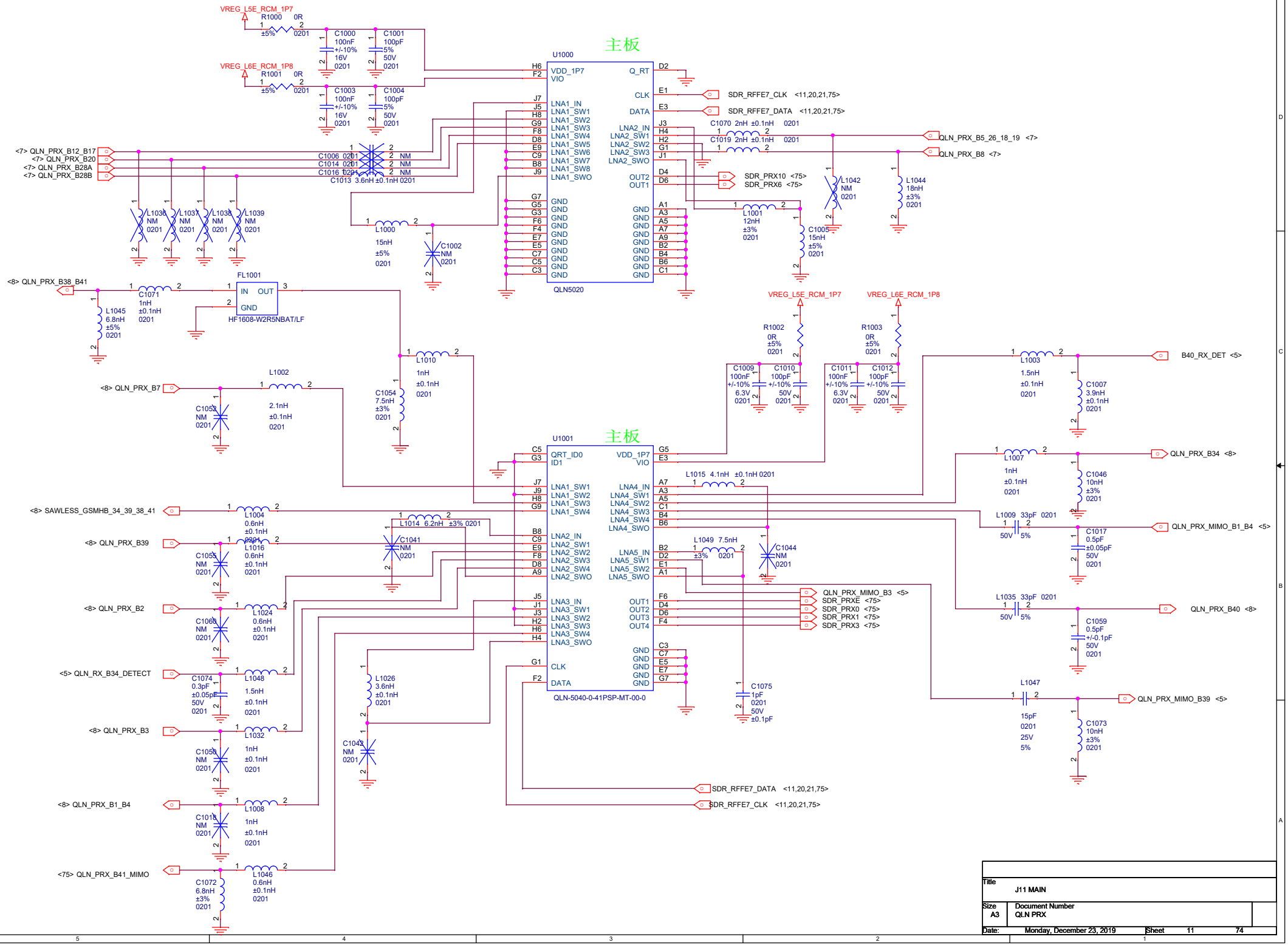
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U1000
QLN5020
主板
U1001
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VREG_L6E_RCM_1P8
SDR_RFFE7_CLK <11,20,21,75>
SDR_RFFE7_DATA <11,20,21,75>
QLN_PRX_B5_26_18_19 <7>
QLN_PRX_B8 <7>
SDR_PRX10 <75>
SDR_PRX6 <75>
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<7> QLN_PRX_B28A
<7> QLN_PRX_B28B
<8> QLN_PRX_B38_B41
HF1608-W2R5NBAT/LF
<8> QLN_PRX_B7
B40_RX_DET <5>
QLN_PRX_B34 <8>
QLN_PRX_MIMO_B1_B4 <5>
QLN_PRX_B40 <8>
QLN_PRX_MIMO_B39 <5>
QLN_PRX_MIMO_B3 <5>
SDR_PRXE <75>
SDR_PRX0 <75>
SDR_PRX1 <75>
SDR_PRX3 <75>
<8> SAWLESS_GSMHB_34_39_38_41
<8> QLN_PRX_B39
<8> QLN_PRX_B2
<5> QLN_RX_B34_DETECT
<8> QLN_PRX_B3
<8> QLN_PRX_B1_B4
<75> QLN_PRX_B41_MIMO
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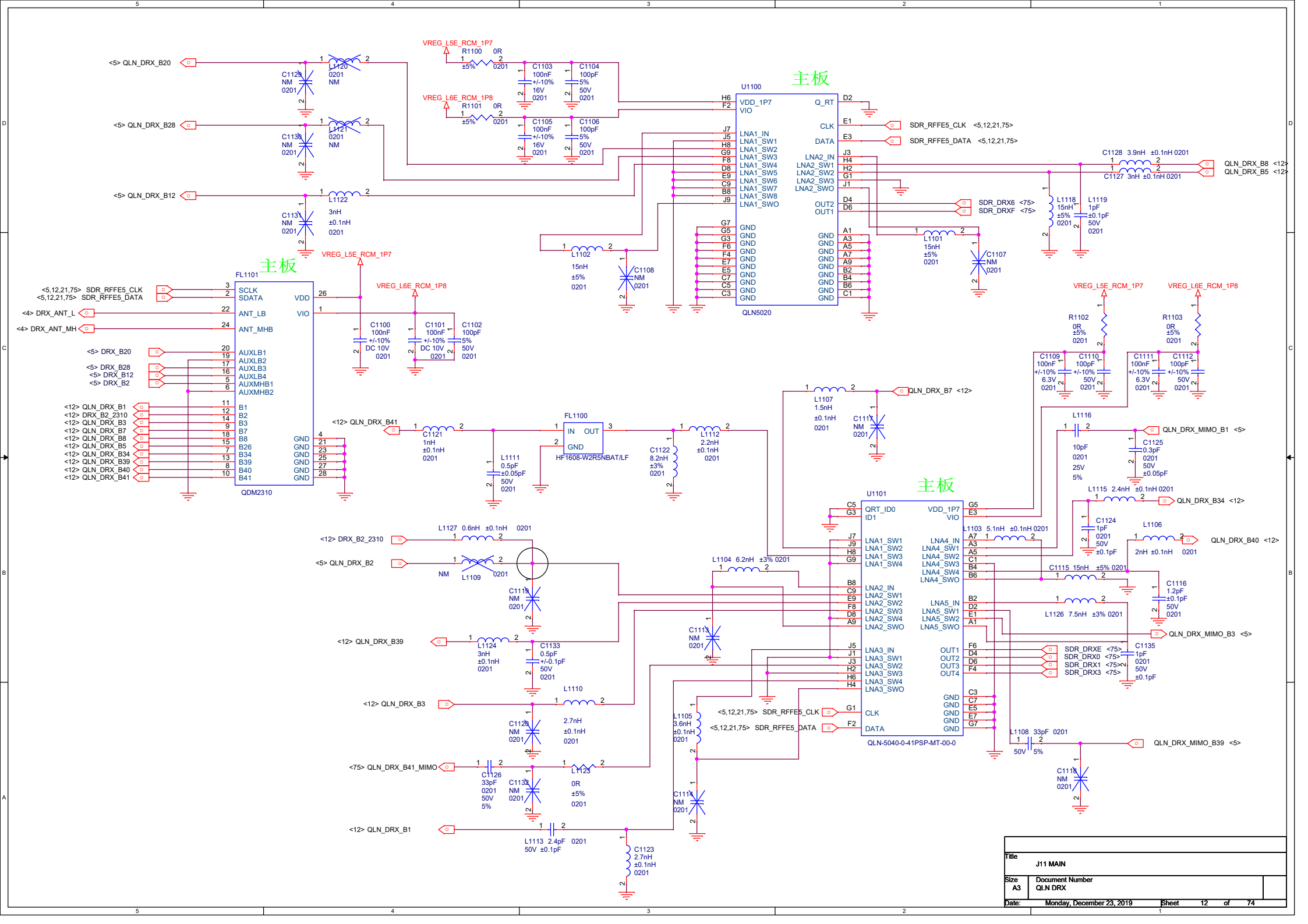
主板
U1100
QLN5020
VREG_L5E_RCM_1P7
VREG_L6E_RCM_1P8
R1100 0R
R1101 0R
C1103 100nF +/-10% 16V 0201
C1104 100pF 5% 50V 0201
C1105 100nF +/-10% 16V 0201
C1106 100pF 5% 50V 0201
<5> QLN_DRX_B20
<5> QLN_DRX_B28
<5> QLN_DRX_B12
L1120 0201 NM
L1121 0201 NM
L1122 3nH ±0.1nH 0201
L1102 15nH ±5% 0201
C1108 NM 0201
L1101 15nH ±5% 0201
C1107 NM 0201
SDR_RFFE5_CLK <5,12,21,75>
SDR_RFFE5_DATA <5,12,21,75>
SDR_DRX6 <75>
SDR_DRXF <75>
C1128 3.9nH ±0.1nH 0201
C1127 3nH ±0.1nH 0201
QLN_DRX_B8 <12>
QLN_DRX_B5 <12>
L1118 15nH ±5% 0201
L1119 1pF ±0.1pF 50V 0201
主板
FL1101
QDM2310
<5,12,21,75> SDR_RFFE5_CLK
<5,12,21,75> SDR_RFFE5_DATA
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<5> DRX_B2
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<12> QLN_DRX_B41
C1100 100nF +/-10% DC 10V 0201
C1101 100nF +/-10% DC 10V 0201
C1102 100pF 5% 50V 0201
R1102 0R ±5% 0201
R1103 0R ±5% 0201
C1109 100nF +/-10% 6.3V 0201
C1110 100pF +/-10% 50V 0201
C1111 100nF +/-10% 6.3V 0201
C1112 100pF +/-10% 50V 0201
L1107 1.5nH ±0.1nH 0201
C1113 NM 0201
L1116
C1125 0.3pF 0201 50V ±0.05pF
10pF 0201 25V 5%
QLN_DRX_MIMO_B1 <5>
L1115 2.4nH ±0.1nH 0201
C1124 1pF 0201 50V ±0.1pF
L1106 2nH ±0.1nH 0201
C1115 15nH ±5% 0201
C1116 1.2pF ±0.1pF 50V 0201
L1126 7.5nH ±3% 0201
QLN_DRX_MIMO_B3 <5>
SDR_DRXE <75>
SDR_DRX0 <75>
SDR_DRX1 <75>
SDR_DRX3 <75>
C1135 1pF 0201 50V ±0.1pF
L1108 33pF 0201 50V 5%
QLN_DRX_MIMO_B39 <5>
C1121 1nH ±0.1nH 0201
FL1100
HF1608-W2R5NBAT/LF
L1111 0.5pF ±0.05pF 50V 0201
C1122 8.2nH ±3% 0201
L1112 2.2nH ±0.1nH 0201
L1127 0.6nH ±0.1nH 0201
L1109 NM 0201
C1119 NM 0201
L1104 6.2nH ±3% 0201
C1111 NM 0201
L1124 3nH ±0.1nH 0201
C1133 0.5pF +/-0.1pF 50V 0201
L1110 2.7nH ±0.1nH 0201
C1120 NM 0201
C1126 33pF 0201 50V 5%
C1132 NM 0201
L1123 0R ±5% 0201
L1105 3.6nH ±0.1nH 0201
C1114 NM 0201
L1113 2.4pF 0201 50V ±0.1pF
C1123 2.7nH ±0.1nH 0201
QLN-5040-0-41PSP-MT-00-0
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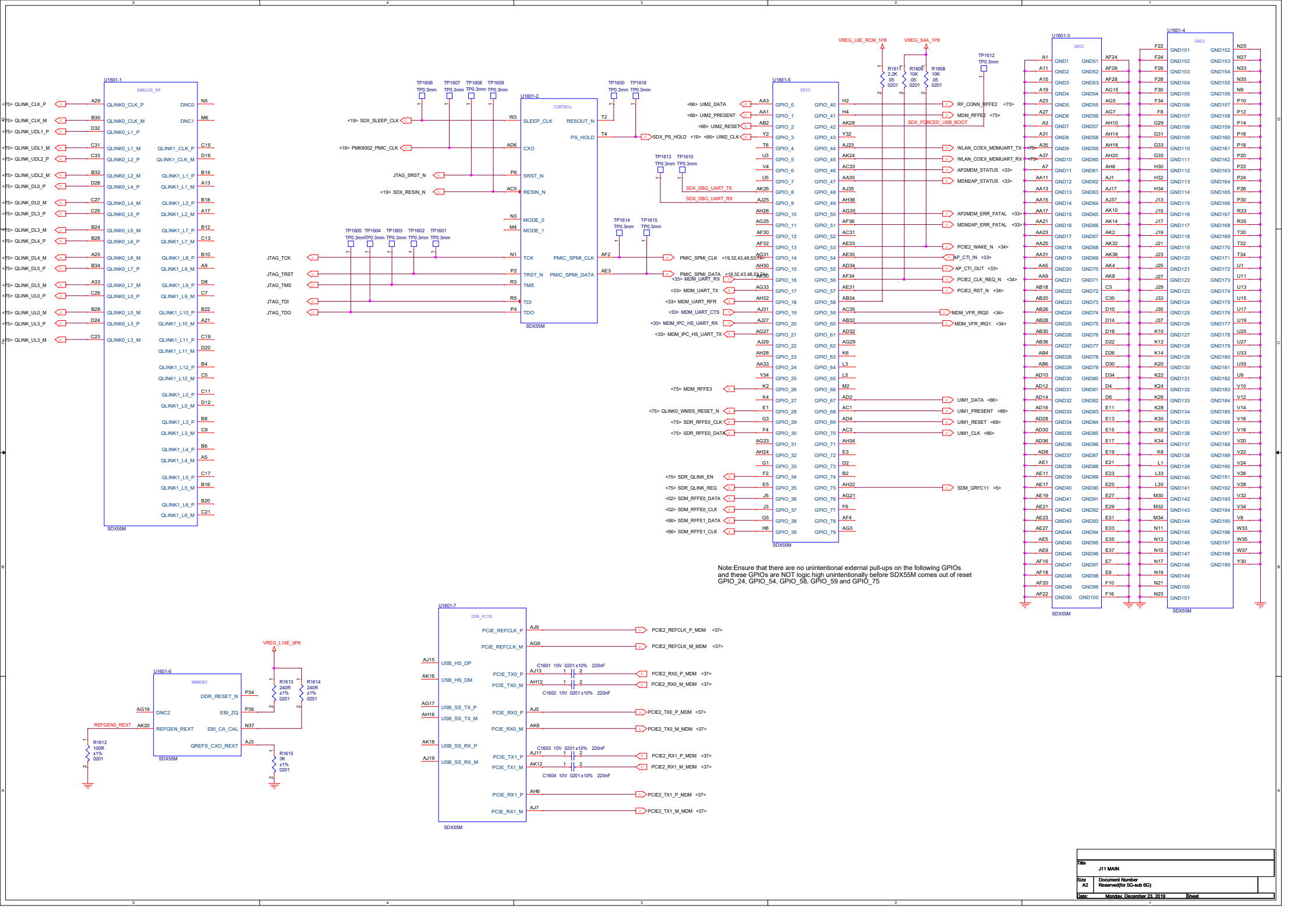
U1601-1
ANALOG_RF
SDX55M
U1601-2
CONTROL
SDX55M
U1601-5
GPIO
SDX55M
U1601-3
GND1
SDX55M
U1601-4
GND2
SDX55M
U1601-6
MEMORY
SDX55M
U1601-7
USB_PCIE
SDX55M
Note:Ensure that there are no unintentional external pull-ups on the following GPIOs and these GPIOs are NOT logic high unintentionally before SDX55M comes out of reset GPIO_24, GPIO_54, GPIO_58, GPIO_59 and GPIO_75
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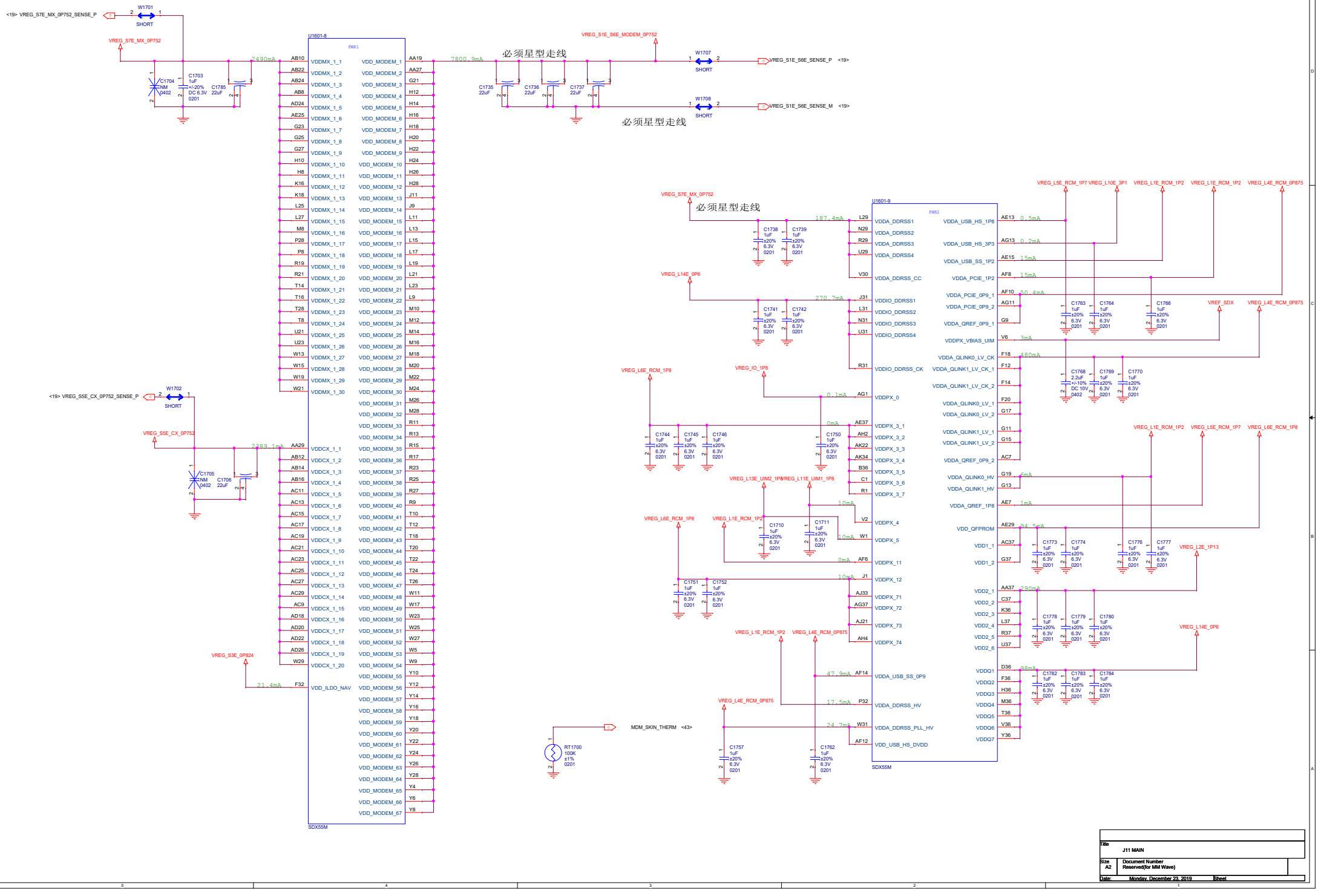
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SHORT
<19> VREG_S7E_MX_0P752_SENSE_P
VREG_S7E_MX_0P752
2490mA
C1703 1uF +/-20% DC 6.3V 0201
C1704 NM 0402
C1785 22uF
U1601-8
PWR1
VDDMX_1_1
VDDMX_1_2
VDDMX_1_3
VDDMX_1_4
VDDMX_1_5
VDDMX_1_6
VDDMX_1_7
VDDMX_1_8
VDDMX_1_9
VDDMX_1_10
VDDMX_1_11
VDDMX_1_12
VDDMX_1_13
VDDMX_1_14
VDDMX_1_15
VDDMX_1_16
VDDMX_1_17
VDDMX_1_18
VDDMX_1_19
VDDMX_1_20
VDDMX_1_21
VDDMX_1_22
VDDMX_1_23
VDDMX_1_24
VDDMX_1_25
VDDMX_1_26
VDDMX_1_27
VDDMX_1_28
VDDMX_1_29
VDDMX_1_30
W1702
SHORT
<19> VREG_S5E_CX_0P752_SENSE_P
VREG_S5E_CX_0P752
2389.1mA
C1705 NM 0402
C1706 22uF
VDDCX_1_1
VDDCX_1_2
VDDCX_1_3
VDDCX_1_4
VDDCX_1_5
VDDCX_1_6
VDDCX_1_7
VDDCX_1_8
VDDCX_1_9
VDDCX_1_10
VDDCX_1_11
VDDCX_1_12
VDDCX_1_13
VDDCX_1_14
VDDCX_1_15
VDDCX_1_16
VDDCX_1_17
VDDCX_1_18
VDDCX_1_19
VDDCX_1_20
VREG_S3E_0P824
21.4mA
VDD_ILDO_NAV
VDD_MODEM_1
VDD_MODEM_2
VDD_MODEM_3
VDD_MODEM_4
VDD_MODEM_5
VDD_MODEM_6
VDD_MODEM_7
VDD_MODEM_8
VDD_MODEM_9
VDD_MODEM_10
VDD_MODEM_11
VDD_MODEM_12
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VDD_MODEM_19
VDD_MODEM_20
VDD_MODEM_21
VDD_MODEM_22
VDD_MODEM_23
VDD_MODEM_24
VDD_MODEM_25
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VDD_MODEM_47
VDD_MODEM_48
VDD_MODEM_49
VDD_MODEM_50
VDD_MODEM_51
VDD_MODEM_52
VDD_MODEM_53
VDD_MODEM_54
VDD_MODEM_55
VDD_MODEM_56
VDD_MODEM_57
VDD_MODEM_58
VDD_MODEM_59
VDD_MODEM_60
VDD_MODEM_61
VDD_MODEM_62
VDD_MODEM_63
VDD_MODEM_64
VDD_MODEM_65
VDD_MODEM_66
VDD_MODEM_67
SDX55M
7800.9mA
必须星型走线
C1735 22uF
C1736 22uF
C1737 22uF
必须星型走线
VREG_S1E_S6E_MODEM_0P752
W1707
SHORT
VREG_S1E_S6E_SENSE_P <19>
W1708
SHORT
VREG_S1E_S6E_SENSE_M <19>
VREG_S7E_MX_0P752
必须星型走线
187.4mA
C1738 1uF ±20% 6.3V 0201
C1739 1uF ±20% 6.3V 0201
VREG_L14E_0P6
270.7mA
C1741 1uF ±20% 6.3V 0201
C1742 1uF ±20% 6.3V 0201
VREG_L6E_RCM_1P8
VREG_IO_1P8
0.1mA
0mA
C1744 1uF ±20% 6.3V 0201
C1745 1uF ±20% 6.3V 0201
C1746 1uF ±20% 6.3V 0201
C1750 1uF ±20% 6.3V 0201
VREG_L13E_UIM2_1P8
VREG_L11E_UIM1_1P8
10mA
C1710 1uF ±20% 6.3V 0201
C1711 1uF ±20% 6.3V 0201
C1751 1uF ±20% 6.3V 0201
C1752 1uF ±20% 6.3V 0201
VREG_L1E_RCM_1P2
VREG_L4E_RCM_0P875
47.9mA
17.5mA
24.7mA
C1757 1uF ±20% 6.3V 0201
C1762 1uF ±20% 6.3V 0201
MDM_SKIN_THERM <43>
RT1700 100K ±1% 0201
U1601-9
PWR2
VDDA_DDRSS1
VDDA_DDRSS2
VDDA_DDRSS3
VDDA_DDRSS4
VDDA_DDRSS_CC
VDDIO_DDRSS1
VDDIO_DDRSS2
VDDIO_DDRSS3
VDDIO_DDRSS4
VDDIO_DDRSS_CK
VDDPX_0
VDDPX_3_1
VDDPX_3_2
VDDPX_3_3
VDDPX_3_4
VDDPX_3_5
VDDPX_3_6
VDDPX_3_7
VDDPX_4
VDDPX_5
VDDPX_11
VDDPX_12
VDDPX_71
VDDPX_72
VDDPX_73
VDDPX_74
VDDA_USB_SS_0P9
VDDA_DDRSS_HV
VDDA_DDRSS_PLL_HV
VDD_USB_HS_DVDD
SDX55M
VDDA_USB_HS_1P8
VDDA_USB_HS_3P3
VDDA_USB_SS_1P2
VDDA_PCIE_1P2
VDDA_PCIE_0P9_1
VDDA_PCIE_0P9_2
VDDA_QREF_0P9_1
VDDPX_VBIAS_UIM
VDDA_QLINK0_LV_CK
VDDA_QLINK1_LV_CK_1
VDDA_QLINK1_LV_CK_2
VDDA_QLINK0_LV_1
VDDA_QLINK0_LV_2
VDDA_QLINK1_LV_1
VDDA_QLINK1_LV_2
VDDA_QREF_0P9_2
VDDA_QLINK0_HV
VDDA_QLINK1_HV
VDDA_QREF_1P8
VDD_QFPROM
VDD1_1
VDD1_2
VDD2_1
VDD2_2
VDD2_3
VDD2_4
VDD2_5
VDD2_6
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
AE13 0.5mA
AG13 0.2mA
AE15 15mA
AF8 15mA
AF10 50.4mA
AG11
G9
V6 3mA
F18 480mA
F12
F14
F20
G17
G11
G15
AC7
G19 6mA
G13
AE7 1mA
AE29 94.5mA
AC37
G37
AA37 290mA
C37
K36
L37
R37
U37
D36 98mA
F36
H36
M36
T36
V36
Y36
VREG_L5E_RCM_1P7
VREG_L10E_3P1
VREG_L1E_RCM_1P2
VREG_L1E_RCM_1P2
VREG_L4E_RCM_0P875
VREF_SDX
VREG_L4E_RCM_0P875
C1763 1uF ±20% 6.3V 0201
C1764 1uF ±20% 6.3V 0201
C1766 1uF ±20% 6.3V 0201
C1768 2.2uF +/-10% DC 10V 0402
C1769 1uF ±20% 6.3V 0201
C1770 1uF ±20% 6.3V 0201
VREG_L1E_RCM_1P2
VREG_L5E_RCM_1P7
VREG_L6E_RCM_1P8
VREG_L2E_1P13
C1773 1uF ±20% 6.3V 0201
C1774 1uF ±20% 6.3V 0201
C1776 1uF ±20% 6.3V 0201
C1777 1uF ±20% 6.3V 0201
C1778 1uF ±20% 6.3V 0201
C1779 1uF ±20% 6.3V 0201
C1780 1uF ±20% 6.3V 0201
VREG_L14E_0P6
C1782 1uF ±20% 6.3V 0201
C1783 1uF ±20% 6.3V 0201
C1784 1uF ±20% 6.3V 0201
Title
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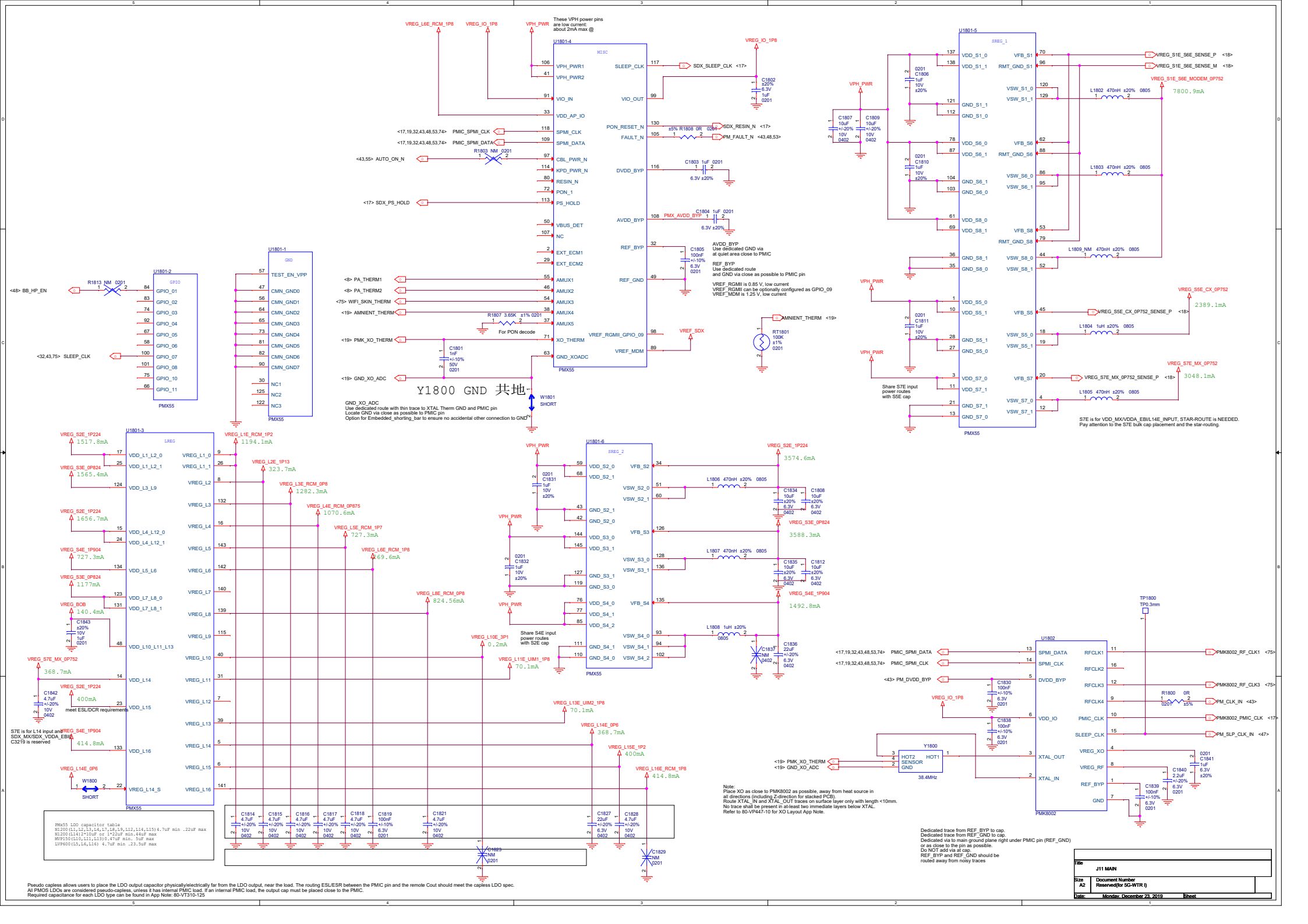
U1801-4
MISC
VREG_L6E_RCM_1P8
VREG_IO_1P8
VPH_PWR
These VPH power pins are low current: about 2mA max @
VPH_PWR1
VPH_PWR2
VIO_IN
VDD_AP_IO
SPMI_CLK
SPMI_DATA
CBL_PWR_N
KPD_PWR_N
RESIN_N
PON_1
PS_HOLD
VBUS_DET
NC
EXT_ECM1
EXT_ECM2
AMUX1
AMUX2
AMUX3
AMUX4
AMUX5
XO_THERM
GND_XOADC
SLEEP_CLK
VIO_OUT
PON_RESET_N
FAULT_N
DVDD_BYP
AVDD_BYP
REF_BYP
REF_GND
VREF_RGMII_GPIO_09
VREF_MDM
PMX55
SDX_SLEEP_CLK <17>
SDX_RESIN_N <17>
PM_FAULT_N <43,48,53>
PMIC_SPMI_CLK
PMIC_SPMI_DATA
AUTO_ON_N
SDX_PS_HOLD
PMX_AVDD_BYP
AVDD_BYP
Use dedicated GND via at quiet area close to PMIC
REF_BYP
Use dedicated route and GND via close as possible to PMIC pin
VREF_RGMII is 0.85 V, low current
VREF_RGMII can be optionally configured as GPIO_09
VREF_MDM is 1.25 V, low current
PA_THERM1
PA_THERM2
WIFI_SKIN_THERM
AMNIENT_THERM
PMK_XO_THERM
GND_XO_ADC
For PON decode
RT1801 100K ±1% 0201
Y1800 GND 共地
W1801 SHORT
GND_XO_ADC
Use dedicated route with thin trace to XTAL Therm GND and PMIC pin
Locate GND via close as possible to PMIC pin
Option for Embedded_shorting_bar to ensure no accidental other connection to GND
U1801-5
SREG_1
VPH_PWR
VDD_S1_0
VDD_S1_1
GND_S1_1
GND_S1_0
VDD_S6_0
VDD_S6_1
GND_S6_1
GND_S6_0
VDD_S8_0
VDD_S8_1
GND_S8_1
GND_S8_0
VDD_S5_0
VDD_S5_1
GND_S5_1
GND_S5_0
VDD_S7_0
VDD_S7_1
GND_S7_1
GND_S7_0
VFB_S1
RMT_GND_S1
VSW_S1_0
VSW_S1_1
VFB_S6
RMT_GND_S6
VSW_S6_0
VSW_S6_1
VFB_S8
RMT_GND_S8
VSW_S8_0
VSW_S8_1
VFB_S5
VSW_S5_0
VSW_S5_1
VFB_S7
VSW_S7_0
VSW_S7_1
PMX55
VREG_S1E_S6E_SENSE_P <18>
VREG_S1E_S6E_SENSE_M <18>
VREG_S1E_S6E_MODEM_0P752
7800.9mA
L1802 470nH ±20% 0805
L1803 470nH ±20% 0805
L1809_NM 470nH ±20% 0805
VREG_S5E_CX_0P752
2389.1mA
VREG_S5E_CX_0P752_SENSE_P <18>
L1804 1uH ±20% 0805
VREG_S7E_MX_0P752
3048.1mA
VREG_S7E_MX_0P752_SENSE_P <18>
L1805 470nH ±20% 0805
Share S7E input power routes with S5E cap
S7E is for VDD_MX/VDDA_EBI/L14E_INPUT, STAR-ROUTE is NEEDED.
Pay attention to the S7E bulk cap placement and the star-routing.
U1801-1
GND
TEST_EN_VPP
CMN_GND0
CMN_GND1
CMN_GND2
CMN_GND3
CMN_GND4
CMN_GND5
CMN_GND6
CMN_GND7
NC1
NC2
NC3
PMX55
U1801-2
GPIO
GPIO_01
GPIO_02
GPIO_03
GPIO_04
GPIO_05
GPIO_06
GPIO_07
GPIO_08
GPIO_10
GPIO_11
PMX55
BB_HP_EN
SLEEP_CLK
U1801-3
LREG
VDD_L1_L2_0
VDD_L1_L2_1
VDD_L3_L9
VDD_L4_L12_0
VDD_L4_L12_1
VDD_L5_L6
VDD_L7_L8_0
VDD_L7_L8_1
VDD_L10_L11_L13
VDD_L14
VDD_L15
VDD_L16
VREG_L14_S
VREG_L1_0
VREG_L1_1
VREG_L2
VREG_L3
VREG_L4
VREG_L5
VREG_L6
VREG_L7
VREG_L8
VREG_L9
VREG_L10
VREG_L11
VREG_L12
VREG_L13
VREG_L14
VREG_L15
VREG_L16
PMX55
VREG_S2E_1P224
1517.8mA
VREG_S3E_0P824
1565.4mA
VREG_S2E_1P224
1656.7mA
VREG_S4E_1P904
727.3mA
VREG_S3E_0P824
1177mA
VREG_BOB
140.4mA
VREG_S7E_MX_0P752
368.7mA
VREG_S2E_1P224
400mA
meet ESL/DCR requirements
VREG_S4E_1P904
414.8mA
VREG_L14E_0P6
S7E is for L14 input and SDX_MX/SDX_VDDA_EBI C3219 is reserved
VREG_L1E_RCM_1P2
1194.1mA
VREG_L2E_1P13
323.7mA
VREG_L3E_RCM_0P8
1282.3mA
VREG_L4E_RCM_0P875
1070.6mA
VREG_L5E_RCM_1P7
727.3mA
VREG_L6E_RCM_1P8
69.6mA
VREG_L8E_RCM_0P8
824.56mA
VREG_L10E_3P1
0.2mA
VREG_L11E_UIM1_1P8
70.1mA
VREG_L13E_UIM2_1P8
70.1mA
VREG_L14E_0P6
368.7mA
VREG_L15E_1P2
400mA
VREG_L16E_RCM_1P8
414.8mA
PMx55 LDO capacitor table
N1200(L1,L2,L3,L4,L7,L8,L9,L12,L14,L15)4.7uF min .22uF max
N1200(L14)2*10uF or 1*22uF min.44uF max
WVP150(L10,L11,L13)0.47uF min. 5uF max
LVP600(L5,L6,L16) 4.7uF min .23.5uF max
Pseudo capless allows users to place the LDO output capacitor physically/electrically far from the LDO output, near the load. The routing ESL/ESR between the PMIC pin and the remote Cout should meet the capless LDO spec.
All PMOS LDOs are considered pseudo-capless, unless it has internal PMIC load. If an internal PMIC load, the output cap must be placed close to the PMIC.
Required capacitance for each LDO type can be found in App Note: 80-VT310-125
U1801-6
SREG_2
VPH_PWR
VDD_S2_0
VDD_S2_1
GND_S2_1
GND_S2_0
VDD_S3_0
VDD_S3_1
GND_S3_1
GND_S3_0
VDD_S4_0
VDD_S4_1
VDD_S4_2
GND_S4_1
GND_S4_0
VFB_S2
VSW_S2_0
VSW_S2_1
VFB_S3
VSW_S3_0
VSW_S3_1
VFB_S4
VSW_S4_0
VSW_S4_1
VSW_S4_2
PMX55
VREG_S2E_1P224
3574.6mA
L1806 470nH ±20% 0805
VREG_S3E_0P824
3588.3mA
L1807 470nH ±20% 0805
VREG_S4E_1P904
1492.8mA
L1808 1uH ±20% 0805
C1837 NM 0402
C1836 22uF +/-20% 6.3V 0402
Share S4E input power routes with S2E cap
U1802
SPMI_DATA
SPMI_CLK
DVDD_BYP
VDD_IO
XTAL_OUT
XTAL_IN
RFCLK1
RFCLK2
RFCLK3
RFCLK4
PMIC_CLK
SLEEP_CLK
VREG_XO
VREG_RF
REF_BYP
GND
PMK8002
PMIC_SPMI_DATA
PMIC_SPMI_CLK
PM_DVDD_BYP
VREG_IO_1P8
Y1800
38.4MHz
XO_THERM
GND_XO_ADC
PMK8002_RF_CLK1 <75>
PMK8002_RF_CLK3 <75>
PM_CLK_IN <43>
PMK8002_PMIC_CLK <17>
PM_SLP_CLK_IN <47>
TP1800
TP0.3mm
Note:
Place XO as close to PMK8002 as possible, away from heat source in all directions (including Z-direction for stacked PCB).
Route XTAL_IN and XTAL_OUT traces on surface layer only with length <10mm.
No trace shall be present in at-least two immediate layers below XTAL.
Refer to 80-VP447-10 for XO Layout App Note.
Dedicated trace from REF_BYP to cap.
Dedicated trace from REF_GND to cap.
Dedicated via to main ground plane right under PMIC pin (REF_GND) or as close to the pin as possible.
Do NOT add via at cap.
REF_BYP and REF_GND should be routed away from noisy traces
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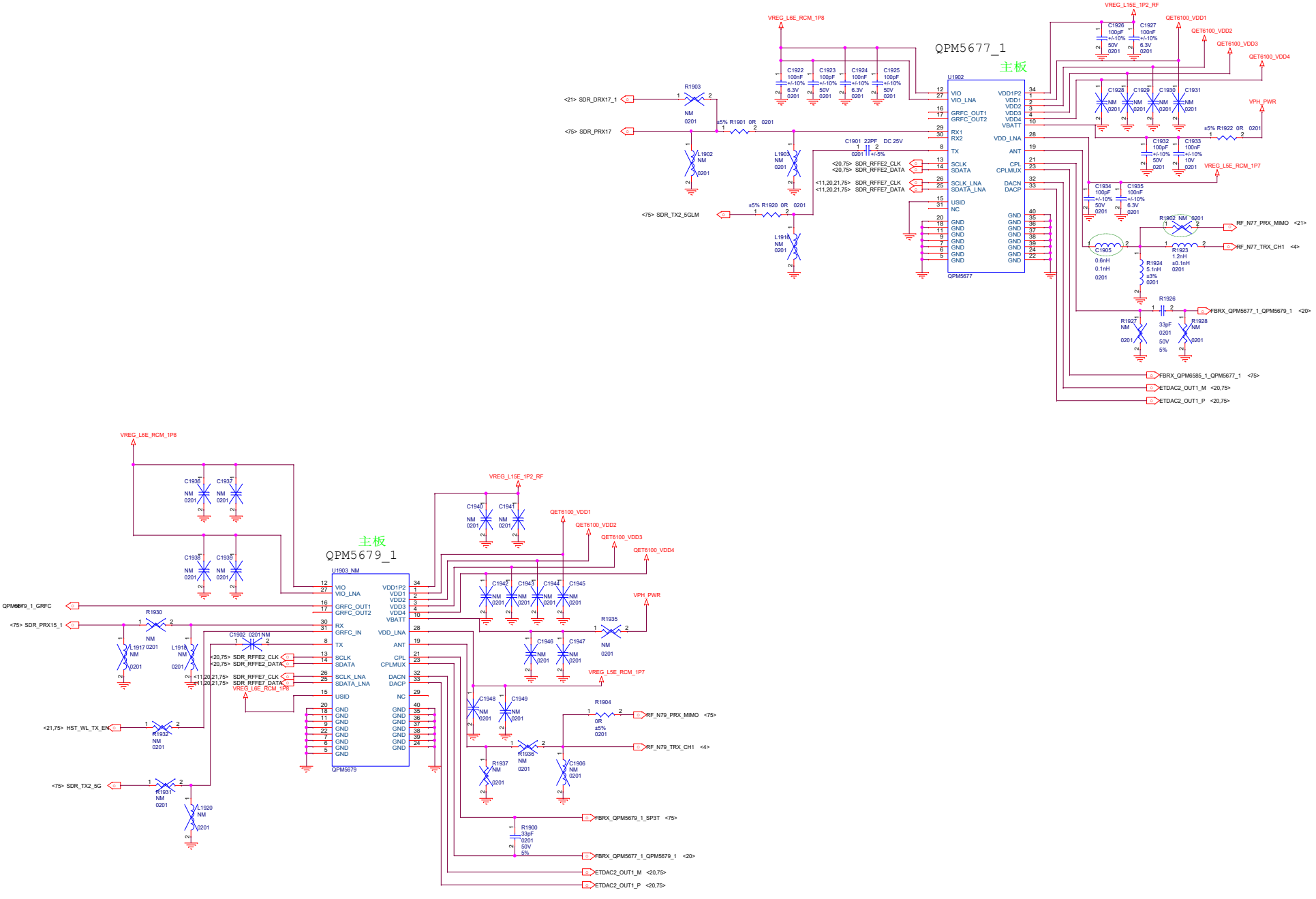

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Size	A2
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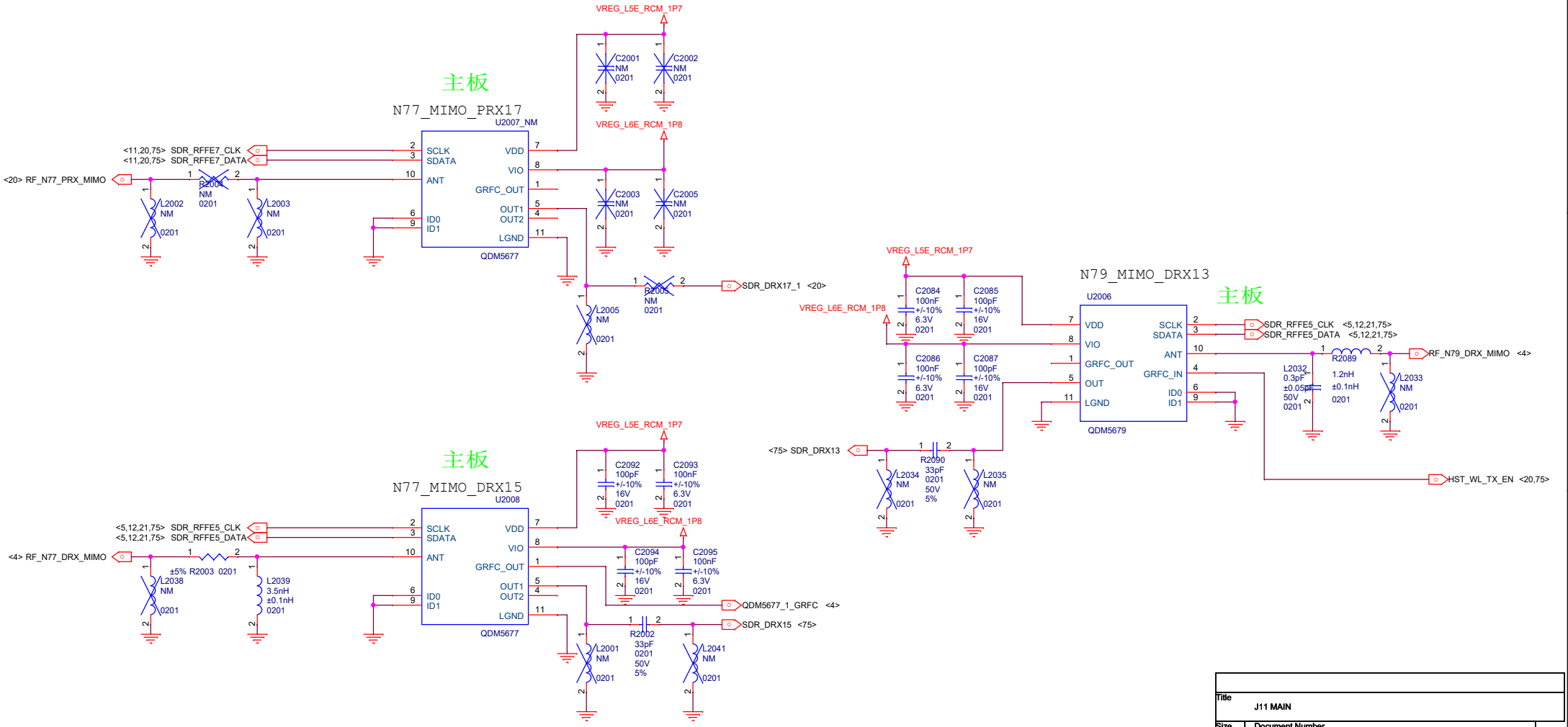

Title	J11 MAIN		
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Size: A2	Document Number: NFC
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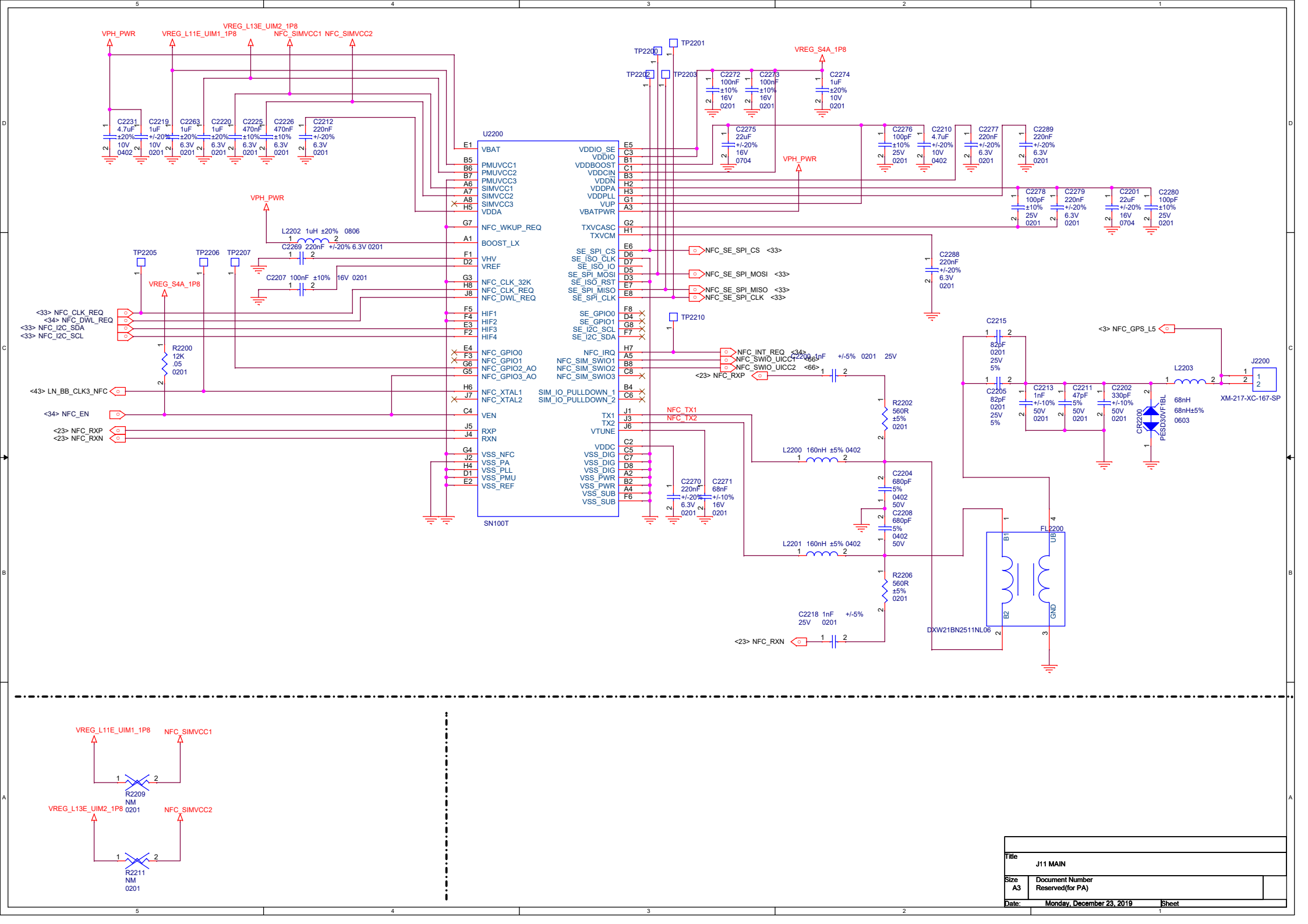
VPH_PWR
VREG_L11E_UIM1_1P8
VREG_L13E_UIM2_1P8
NFC_SIMVCC1
NFC_SIMVCC2
U2200
SN100T
VBAT
PMUVCC1
PMUVCC2
PMUVCC3
SIMVCC1
SIMVCC2
SIMVCC3
VDDA
NFC_WKUP_REQ
BOOST_LX
VHV
VREF
NFC_CLK_32K
NFC_CLK_REQ
NFC_DWL_REQ
HIF1
HIF2
HIF3
HIF4
NFC_GPIO0
NFC_GPIO1
NFC_GPIO2_AO
NFC_GPIO3_AO
NFC_XTAL1
NFC_XTAL2
VEN
RXP
RXN
VSS_NFC
VSS_PA
VSS_PLL
VSS_PMU
VSS_REF
VDDIO_SE
VDDIO
VDDBOOST
VDDCIN
VDDN
VDDPA
VDDPLL
VUP
VBATPWR
TXVCASC
TXVCM
SE_SPI_CS
SE_ISO_CLK
SE_ISO_IO
SE_SPI_MOSI
SE_ISO_RST
SE_SPI_MISO
SE_SPI_CLK
SE_GPIO0
SE_GPIO1
SE_I2C_SCL
SE_I2C_SDA
NFC_IRQ
NFC_SIM_SWIO1
NFC_SIM_SWIO2
NFC_SIM_SWIO3
SIM_IO_PULLDOWN_1
SIM_IO_PULLDOWN_2
TX1
TX2
VTUNE
VDDC
VSS_DIG
VSS_PWR
VSS_SUB
TP2200
TP2201
TP2202
TP2203
TP2205
TP2206
TP2207
TP2210
VREG_S4A_1P8
L2202 1uH ±20% 0806
C2269 220nF +/-20% 6.3V 0201
C2207 100nF ±10% 16V 0201
R2200 12K .05 0201
C2231 4.7uF ±20% 10V 0402
C2219 1uF +/-20% 10V 0201
C2263 1uF ±20% 6.3V 0201
C2220 1uF ±20% 6.3V 0201
C2225 470nF ±10% 6.3V 0201
C2226 470nF ±10% 6.3V 0201
C2212 220nF +/-20% 6.3V 0201
C2272 100nF ±10% 16V 0201
C2273 100nF ±10% 16V 0201
C2274 1uF ±20% 10V 0201
C2275 22uF +/-20% 16V 0704
C2276 100pF ±10% 25V 0201
C2210 4.7uF +/-20% 10V 0402
C2277 220nF +/-20% 6.3V 0201
C2289 220nF +/-20% 6.3V 0201
C2278 100pF ±10% 25V 0201
C2279 220nF +/-20% 6.3V 0201
C2201 22uF +/-20% 16V 0704
C2280 100pF ±10% 25V 0201
C2288 220nF +/-20% 6.3V 0201
C2270 220nF +/-20% 6.3V 0201
C2271 68nF +/-10% 16V 0201
C2200 1nF +/-5% 0201 25V
C2215 82pF 0201 25V 5%
C2205 82pF 0201 25V 5%
C2213 1nF +/-10% 50V 0201
C2211 47pF 5% 50V 0201
C2202 330pF +/-10% 50V 0201
L2203 68nH 68nH±5% 0603
J2200 XM-217-XC-167-SP
CR2200 PESD30VF1BL
R2202 560R ±5% 0201
R2206 560R ±5% 0201
L2200 160nH ±5% 0402
L2201 160nH ±5% 0402
C2204 680pF 5% 0402 50V
C2208 680pF 5% 0402 50V
C2218 1nF +/-5% 25V 0201
FL2200 DXW21BN2511NL06
R2209 NM 0201
R2211 NM 0201
NFC_SE_SPI_CS <33>
NFC_SE_SPI_MOSI <33>
NFC_SE_SPI_MISO <33>
NFC_SE_SPI_CLK <33>
NFC_INT_REQ <34>
NFC_SWIO_UICC1 <66>
NFC_SWIO_UICC2 <66>
<23> NFC_RXP
<23> NFC_RXN
<33> NFC_CLK_REQ
<34> NFC_DWL_REQ
<33> NFC_I2C_SDA
<33> NFC_I2C_SCL
<43> LN_BB_CLK3_NFC
<34> NFC_EN
<3> NFC_GPS_L5
NFC_TX1
NFC_TX2
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Title	J11 MAIN
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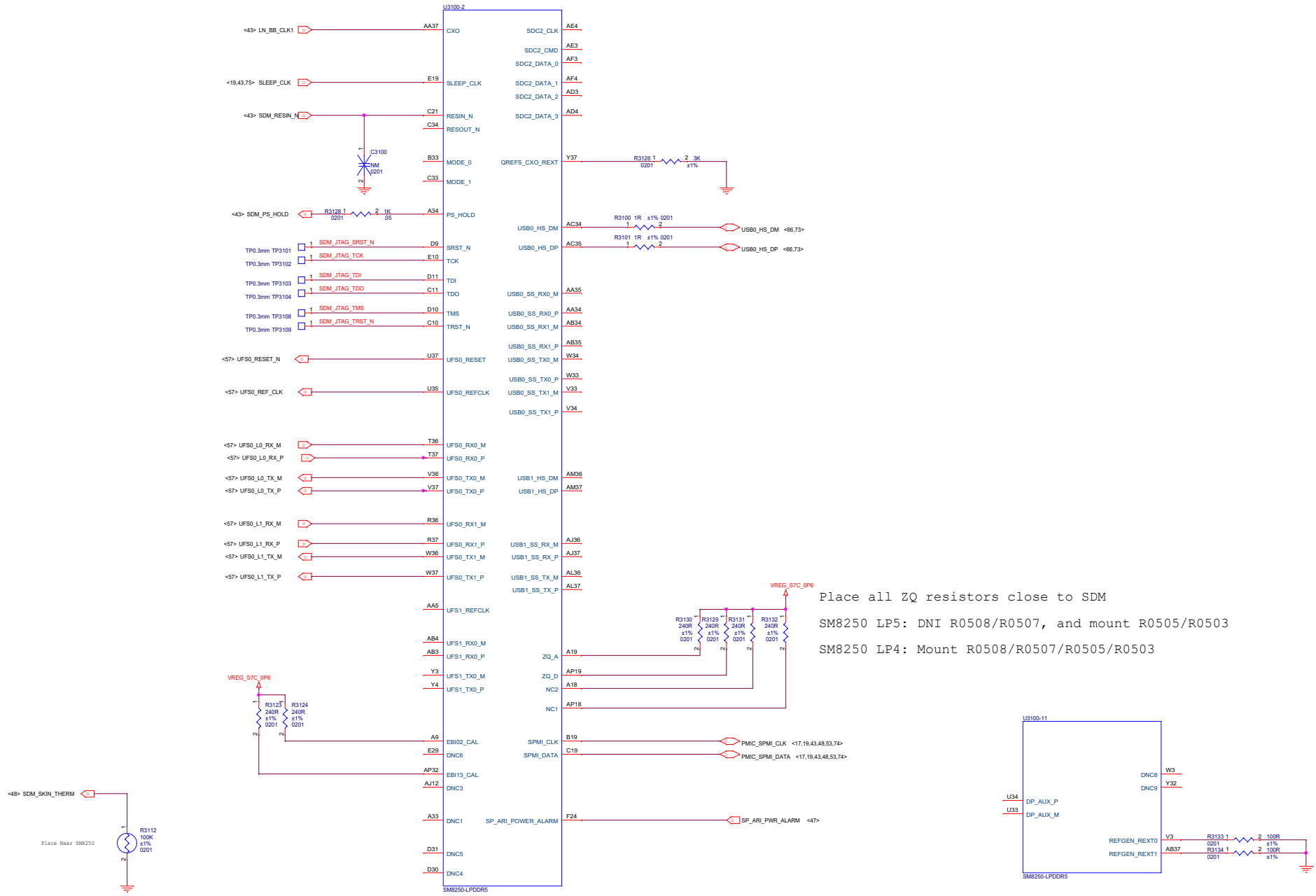
We use current SM8250 symbol as LP5 PKG, and it can be compatible with LP4x PKG



Place all ZQ resistors close to SDM

SM8250 LP5: DNI R0508/R0507, and mount R0505/R0503

SM8250 LP4: Mount R0508/R0507/R0505/R0503

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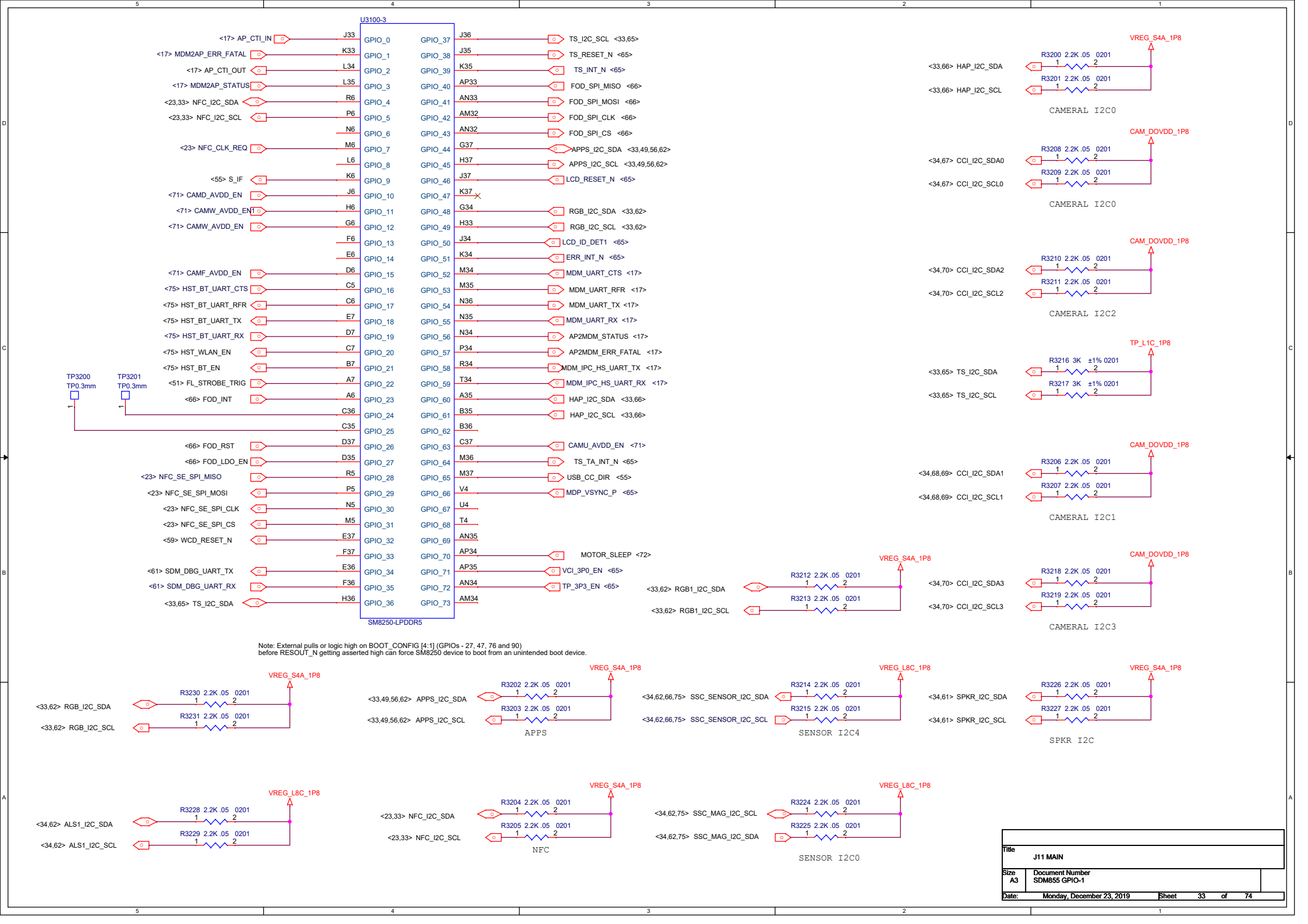
U3100-3
<17> AP_CTI_IN
<17> MDM2AP_ERR_FATAL
<17> AP_CTI_OUT
<17> MDM2AP_STATUS
<23,33> NFC_I2C_SDA
<23,33> NFC_I2C_SCL
<23> NFC_CLK_REQ
<55> S_IF
<71> CAMD_AVDD_EN
<71> CAMW_AVDD_EN1
<71> CAMW_AVDD_EN
<71> CAMF_AVDD_EN
<75> HST_BT_UART_CTS
<75> HST_BT_UART_RFR
<75> HST_BT_UART_TX
<75> HST_BT_UART_RX
<75> HST_WLAN_EN
<75> HST_BT_EN
<51> FL_STROBE_TRIG
<66> FOD_INT
<66> FOD_RST
<66> FOD_LDO_EN
<23> NFC_SE_SPI_MISO
<23> NFC_SE_SPI_MOSI
<23> NFC_SE_SPI_CLK
<23> NFC_SE_SPI_CS
<59> WCD_RESET_N
<61> SDM_DBG_UART_TX
<61> SDM_DBG_UART_RX
<33,65> TS_I2C_SDA
TP3200 TP0.3mm
TP3201 TP0.3mm
GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7 GPIO_8 GPIO_9 GPIO_10 GPIO_11 GPIO_12 GPIO_13 GPIO_14 GPIO_15 GPIO_16 GPIO_17 GPIO_18 GPIO_19 GPIO_20 GPIO_21 GPIO_22 GPIO_23 GPIO_24 GPIO_25 GPIO_26 GPIO_27 GPIO_28 GPIO_29 GPIO_30 GPIO_31 GPIO_32 GPIO_33 GPIO_34 GPIO_35 GPIO_36
GPIO_37 GPIO_38 GPIO_39 GPIO_40 GPIO_41 GPIO_42 GPIO_43 GPIO_44 GPIO_45 GPIO_46 GPIO_47 GPIO_48 GPIO_49 GPIO_50 GPIO_51 GPIO_52 GPIO_53 GPIO_54 GPIO_55 GPIO_56 GPIO_57 GPIO_58 GPIO_59 GPIO_60 GPIO_61 GPIO_62 GPIO_63 GPIO_64 GPIO_65 GPIO_66 GPIO_67 GPIO_68 GPIO_69 GPIO_70 GPIO_71 GPIO_72 GPIO_73
TS_I2C_SCL <33,65>
TS_RESET_N <65>
TS_INT_N <65>
FOD_SPI_MISO <66>
FOD_SPI_MOSI <66>
FOD_SPI_CLK <66>
FOD_SPI_CS <66>
APPS_I2C_SDA <33,49,56,62>
APPS_I2C_SCL <33,49,56,62>
LCD_RESET_N <65>
RGB_I2C_SDA <33,62>
RGB_I2C_SCL <33,62>
LCD_ID_DET1 <65>
ERR_INT_N <65>
MDM_UART_CTS <17>
MDM_UART_RFR <17>
MDM_UART_TX <17>
MDM_UART_RX <17>
AP2MDM_STATUS <17>
AP2MDM_ERR_FATAL <17>
MDM_IPC_HS_UART_TX <17>
MDM_IPC_HS_UART_RX <17>
HAP_I2C_SDA <33,66>
HAP_I2C_SCL <33,66>
CAMU_AVDD_EN <71>
TS_TA_INT_N <65>
USB_CC_DIR <55>
MDP_VSYNC_P <65>
MOTOR_SLEEP <72>
VCI_3P0_EN <65>
TP_3P3_EN <65>
SM8250-LPDDR5
Note: External pulls or logic high on BOOT_CONFIG [4:1] (GPIOs - 27, 47, 76 and 90)
before RESOUT_N getting asserted high can force SM8250 device to boot from an unintended boot device.
VREG_S4A_1P8
<33,66> HAP_I2C_SDA
<33,66> HAP_I2C_SCL
R3200 2.2K .05 0201
R3201 2.2K .05 0201
CAMERAL I2C0
CAM_DOVDD_1P8
<34,67> CCI_I2C_SDA0
<34,67> CCI_I2C_SCL0
R3208 2.2K .05 0201
R3209 2.2K .05 0201
CAMERAL I2C0
<34,70> CCI_I2C_SDA2
<34,70> CCI_I2C_SCL2
R3210 2.2K .05 0201
R3211 2.2K .05 0201
CAMERAL I2C2
TP_L1C_1P8
<33,65> TS_I2C_SDA
<33,65> TS_I2C_SCL
R3216 3K ±1% 0201
R3217 3K ±1% 0201
<34,68,69> CCI_I2C_SDA1
<34,68,69> CCI_I2C_SCL1
R3206 2.2K .05 0201
R3207 2.2K .05 0201
CAMERAL I2C1
<33,62> RGB1_I2C_SDA
<33,62> RGB1_I2C_SCL
R3212 2.2K .05 0201
R3213 2.2K .05 0201
<34,70> CCI_I2C_SDA3
<34,70> CCI_I2C_SCL3
R3218 2.2K .05 0201
R3219 2.2K .05 0201
CAMERAL I2C3
<33,62> RGB_I2C_SDA
<33,62> RGB_I2C_SCL
R3230 2.2K .05 0201
R3231 2.2K .05 0201
<33,49,56,62> APPS_I2C_SDA
<33,49,56,62> APPS_I2C_SCL
R3202 2.2K .05 0201
R3203 2.2K .05 0201
APPS
<34,62,66,75> SSC_SENSOR_I2C_SDA
<34,62,66,75> SSC_SENSOR_I2C_SCL
R3214 2.2K .05 0201
R3215 2.2K .05 0201
SENSOR I2C4
<34,61> SPKR_I2C_SDA
<34,61> SPKR_I2C_SCL
R3226 2.2K .05 0201
R3227 2.2K .05 0201
SPKR I2C
<34,62> ALS1_I2C_SDA
<34,62> ALS1_I2C_SCL
R3228 2.2K .05 0201
R3229 2.2K .05 0201
<23,33> NFC_I2C_SDA
<23,33> NFC_I2C_SCL
R3204 2.2K .05 0201
R3205 2.2K .05 0201
NFC
<34,62,75> SSC_MAG_I2C_SCL
<34,62,75> SSC_MAG_I2C_SDA
R3224 2.2K .05 0201
R3225 2.2K .05 0201
SENSOR I2C0
Title
J11 MAIN
Size A3
Document Number SDM855 GPIO-1
Date: Monday, December 23, 2019
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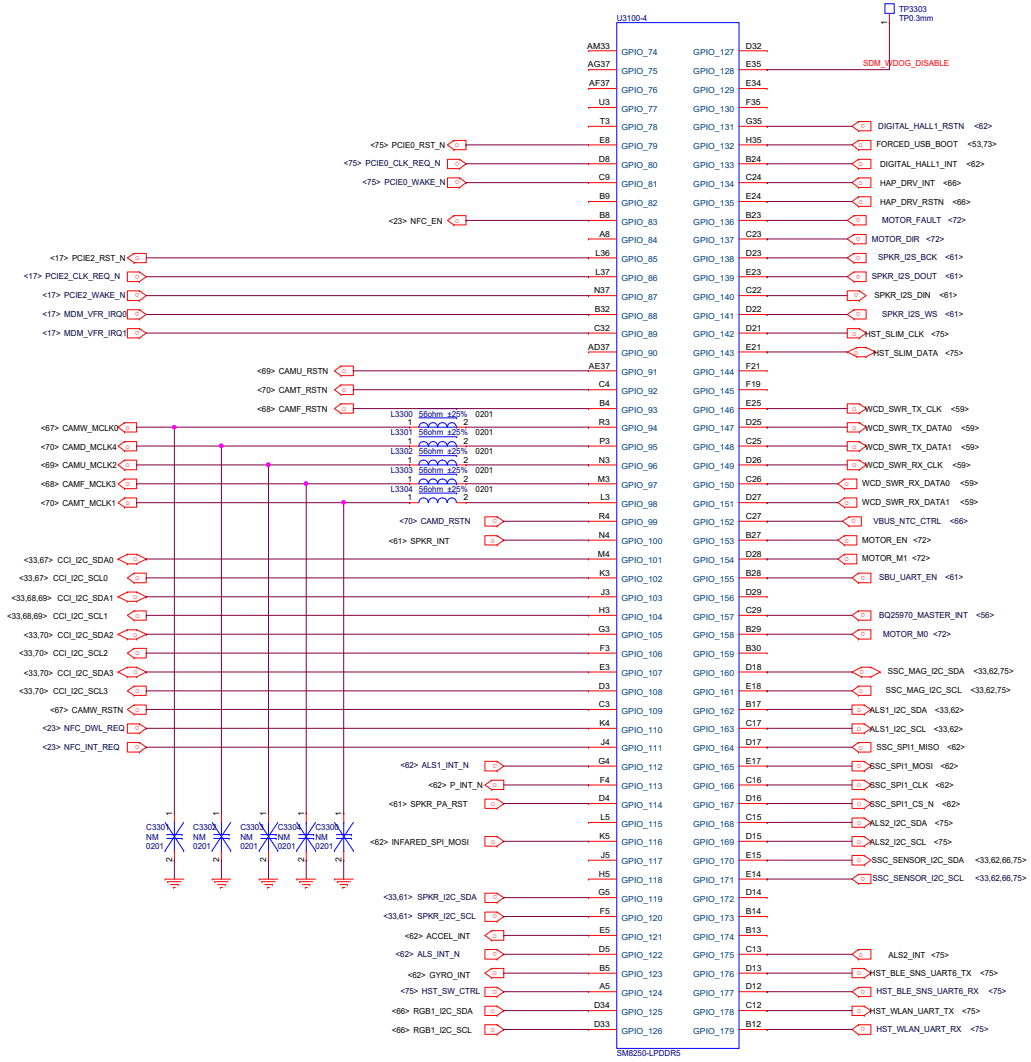
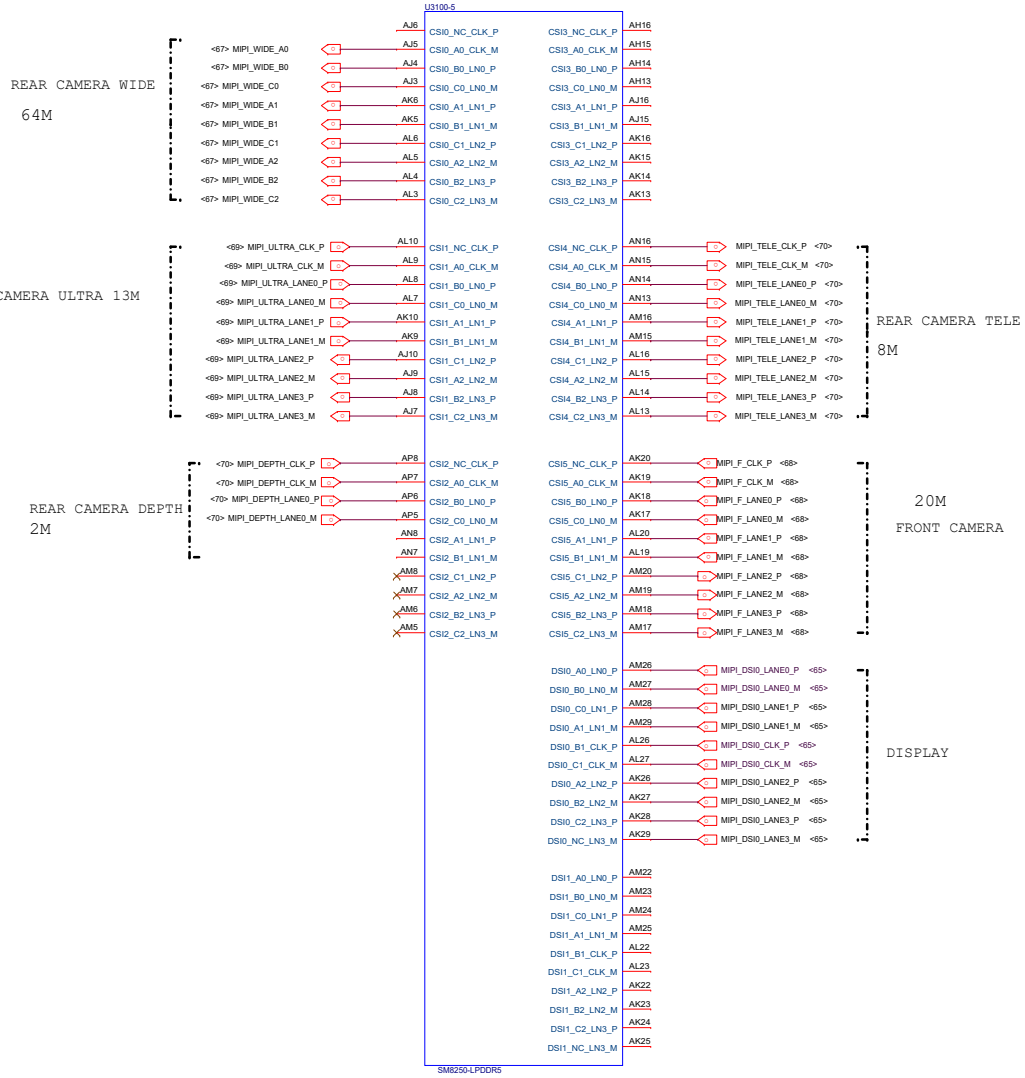


GPIO_128	BOOT_CONFIG(0)	WDOG_DISABLE
GPIO_27	BOOT_CONFIG(1)	FASTBOOT_SEL(0)
GPIO_47	BOOT_CONFIG(2)	FASTBOOT_SEL(1)
GPIO_76	BOOT_CONFIG(3)	FASTBOOT_SEL(2)
GPIO_90	BOOT_CONFIG(4)	FASTBOOT_SEL(3)
GPIO_70	BOOT_CONFIG(5)	APPS_BOOT_FROM_ROM
GPIO_132	N/A	FORCE_USB_BOOT

Title	J11 MAIN	
Size A2	Document Number SDM855 GPIO-2	
Date: Monday, December 23, 2019	Sheet	



Title	J11 MAIN	
Size A2	Document Number SDM855 MIPI	
Date: Monday, December 23, 2019	Sheet	

Title	J11 MAIN
Size: A4	Document Number: Reserved(for MIPI)
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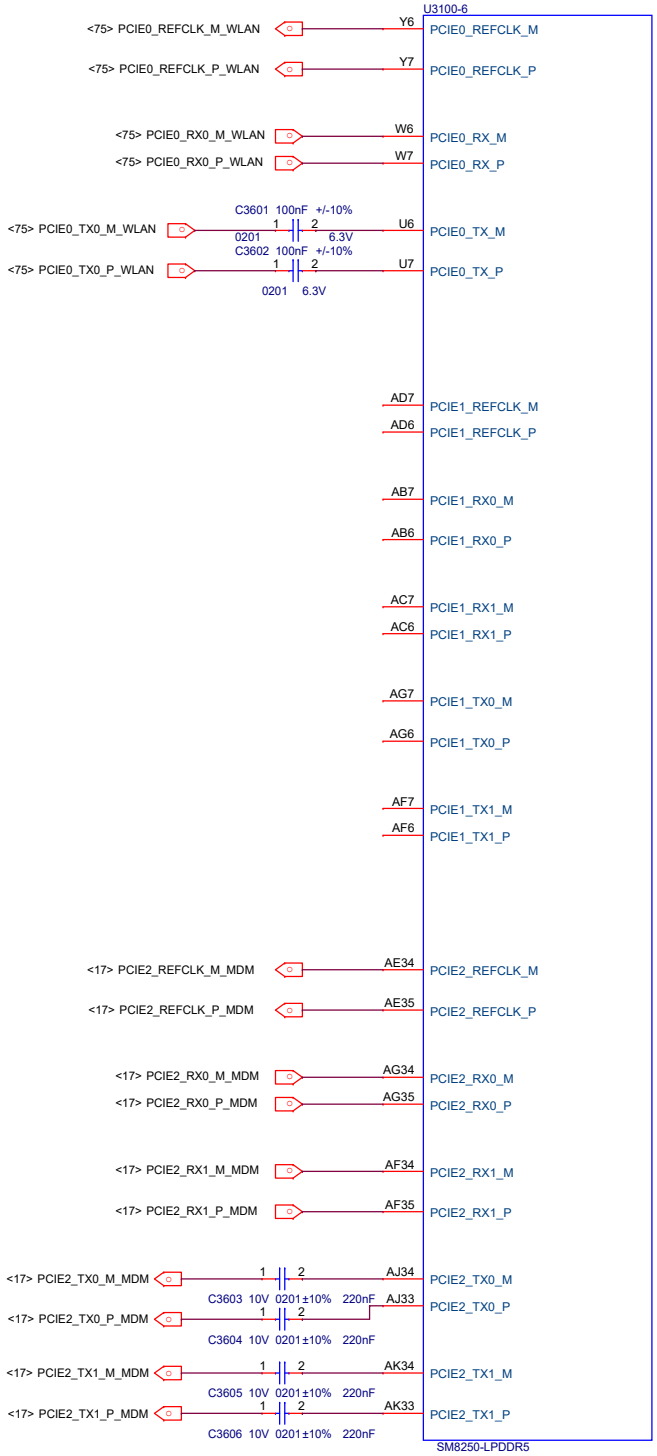
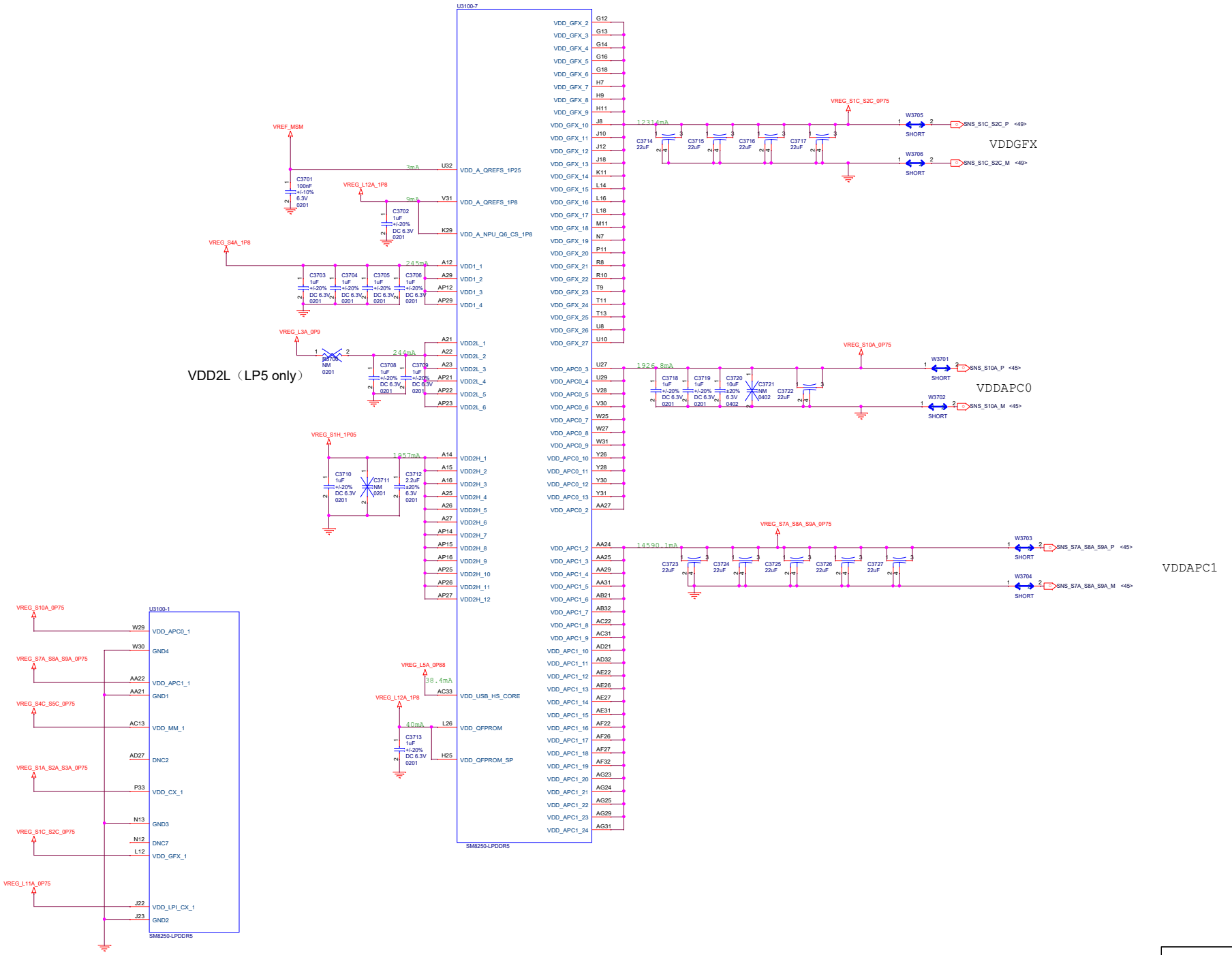
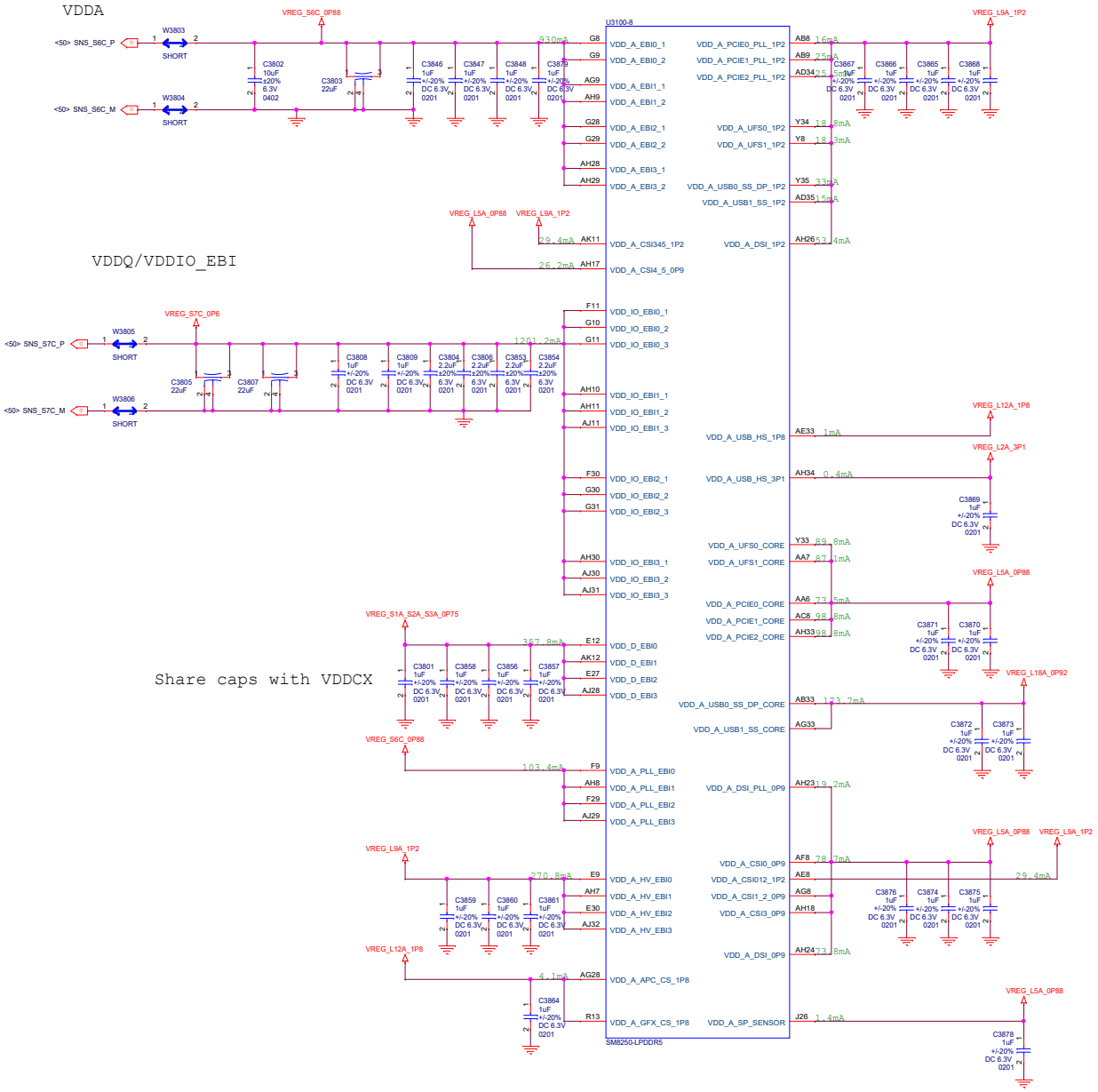
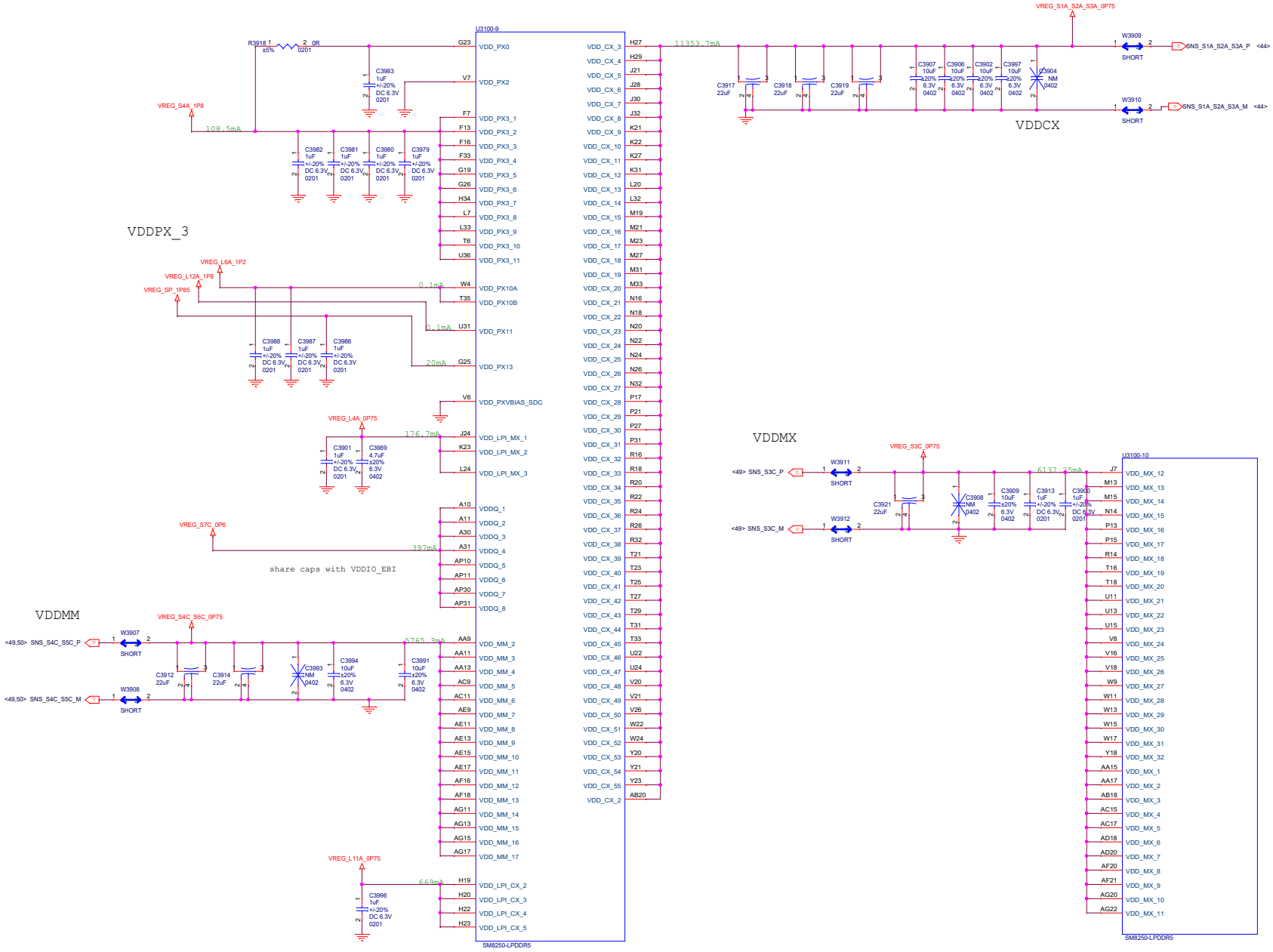


Title	J11 MAIN
Size	A3
Document Number	SDM855 RF INTF
Date:	Monday, December 23, 2019
Sheet	37 74


U3100-7
VREF_MSM
C3701 100nF +/-10% 6.3V 0201
VREG_L12A_1P8
C3702 1uF +/-20% DC 6.3V 0201
3mA
9mA
U32
V31
K29
VDD_A_QREFS_1P25
VDD_A_QREFS_1P8
VDD_A_NPU_Q6_CS_1P8
VREG_S4A_1P8
C3703 1uF +/-20% DC 6.3V 0201
C3704 1uF +/-20% DC 6.3V 0201
C3705 1uF +/-20% DC 6.3V 0201
C3706 1uF +/-20% DC 6.3V 0201
245mA
A12
A29
AP12
AP29
VDD1_1
VDD1_2
VDD1_3
VDD1_4
VREG_L3A_0P9
C3708 1uF +/-20% DC 6.3V 0201
C3709 1uF +/-20% DC 6.3V 0201
244mA
A21
A22
A23
AP21
AP22
AP23
VDD2L_1
VDD2L_2
VDD2L_3
VDD2L_4
VDD2L_5
VDD2L_6
VDD2L（LP5 only）
VREG_S1H_1P05
C3710 1uF +/-20% DC 6.3V 0201
C3711 NM 0201
C3712 2.2uF ±20% 6.3V 0201
1957mA
A14
A15
A16
A25
A26
A27
AP14
AP15
AP16
AP25
AP26
AP27
VDD2H_1
VDD2H_2
VDD2H_3
VDD2H_4
VDD2H_5
VDD2H_6
VDD2H_7
VDD2H_8
VDD2H_9
VDD2H_10
VDD2H_11
VDD2H_12
VREG_L5A_0P88
38.4mA
AC33
VDD_USB_HS_CORE
VREG_L12A_1P8
C3713 1uF +/-20% DC 6.3V 0201
40mA
L26
H25
VDD_QFPROM
VDD_QFPROM_SP
SM8250-LPDDR5
VDD_GFX_2 G12
VDD_GFX_3 G13
VDD_GFX_4 G14
VDD_GFX_5 G16
VDD_GFX_6 G18
VDD_GFX_7 H7
VDD_GFX_8 H9
VDD_GFX_9 H11
VDD_GFX_10 J8
VDD_GFX_11 J10
VDD_GFX_12 J12
VDD_GFX_13 J18
VDD_GFX_14 K11
VDD_GFX_15 L14
VDD_GFX_16 L16
VDD_GFX_17 L18
VDD_GFX_18 M11
VDD_GFX_19 N7
VDD_GFX_20 P11
VDD_GFX_21 R8
VDD_GFX_22 R10
VDD_GFX_23 T9
VDD_GFX_24 T11
VDD_GFX_25 T13
VDD_GFX_26 U8
VDD_GFX_27 U10
VREG_S1C_S2C_0P75
12314mA
C3714 22uF
C3715 22uF
C3716 22uF
C3717 22uF
W3705 SHORT
W3706 SHORT
SNS_S1C_S2C_P <49>
SNS_S1C_S2C_M <49>
VDDGFX
VDD_APC0_3 U27
VDD_APC0_4 U29
VDD_APC0_5 V28
VDD_APC0_6 V30
VDD_APC0_7 W25
VDD_APC0_8 W27
VDD_APC0_9 W31
VDD_APC0_10 Y26
VDD_APC0_11 Y28
VDD_APC0_12 Y30
VDD_APC0_13 Y31
VDD_APC0_2 AA27
VREG_S10A_0P75
1926.8mA
C3718 1uF +/-20% DC 6.3V 0201
C3719 1uF +/-20% DC 6.3V 0201
C3720 10uF ±20% 6.3V 0402
C3721 NM 0402
C3722 22uF
W3701 SHORT
W3702 SHORT
SNS_S10A_P <45>
SNS_S10A_M <45>
VDDAPC0
VDD_APC1_2 AA24
VDD_APC1_3 AA25
VDD_APC1_4 AA29
VDD_APC1_5 AA31
VDD_APC1_6 AB21
VDD_APC1_7 AB32
VDD_APC1_8 AC22
VDD_APC1_9 AC31
VDD_APC1_10 AD21
VDD_APC1_11 AD32
VDD_APC1_12 AE22
VDD_APC1_13 AE26
VDD_APC1_14 AE27
VDD_APC1_15 AE31
VDD_APC1_16 AF22
VDD_APC1_17 AF26
VDD_APC1_18 AF27
VDD_APC1_19 AF32
VDD_APC1_20 AG23
VDD_APC1_21 AG24
VDD_APC1_22 AG25
VDD_APC1_23 AG29
VDD_APC1_24 AG31
VREG_S7A_S8A_S9A_0P75
14590.1mA
C3723 22uF
C3724 22uF
C3725 22uF
C3726 22uF
C3727 22uF
W3703 SHORT
W3704 SHORT
SNS_S7A_S8A_S9A_P <45>
SNS_S7A_S8A_S9A_M <45>
VDDAPC1
VREG_S10A_0P75
VREG_S7A_S8A_S9A_0P75
VREG_S4C_S5C_0P75
VREG_S1A_S2A_S3A_0P75
VREG_S1C_S2C_0P75
VREG_L11A_0P75
U3100-1
W29 VDD_APC0_1
W30 GND4
AA22 VDD_APC1_1
AA21 GND1
AC13 VDD_MM_1
AD27 DNC2
P33 VDD_CX_1
N13 GND3
N12 DNC7
L12 VDD_GFX_1
J22 VDD_LPI_CX_1
J23 GND2
SM8250-LPDDR5
Title
J11 MAIN
Size A2
Document Number SDM8SS PWR1
Date: Monday, December 23, 2019
Sheet

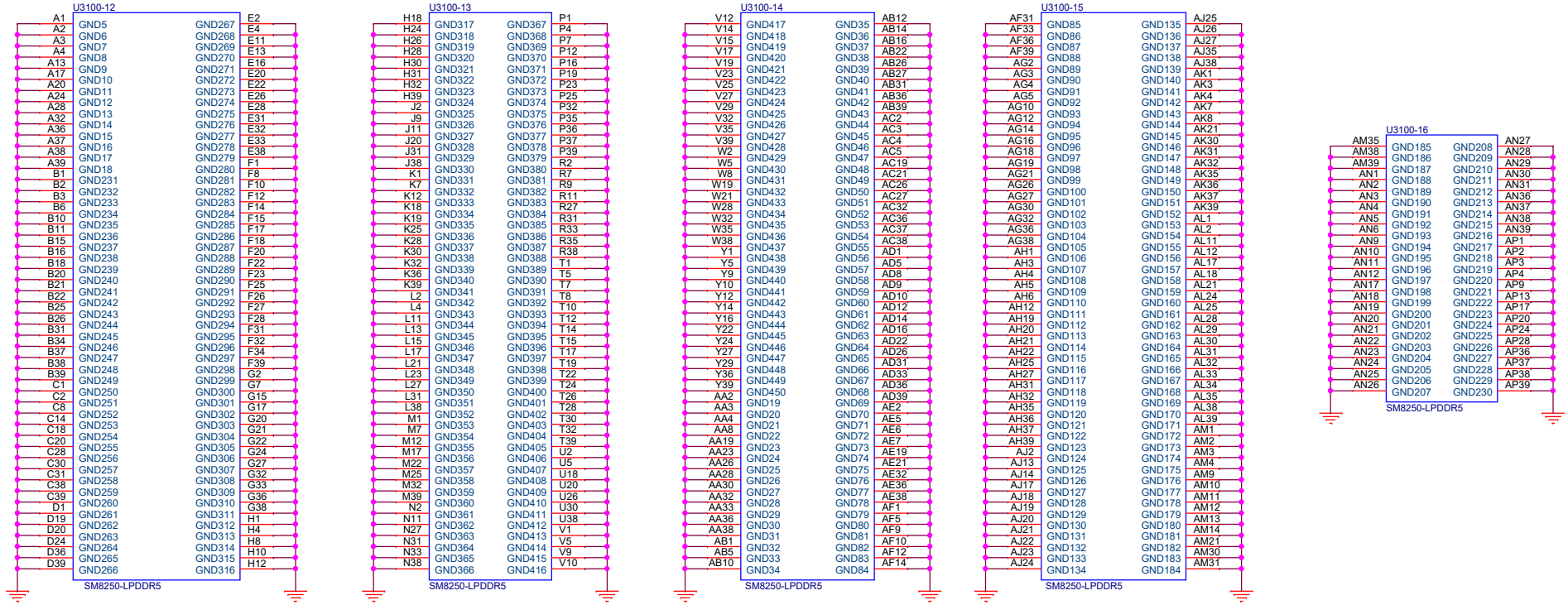


Title	J11 MAIN	
Size A2	Document Number SDM8SS PWR2	
Date: Monday, December 23, 2019	Sheet	



Title	J11 MAIN	
Size A2	Document Number SDM855 PWR3	
Date: Monday, December 23, 2019	Sheet	

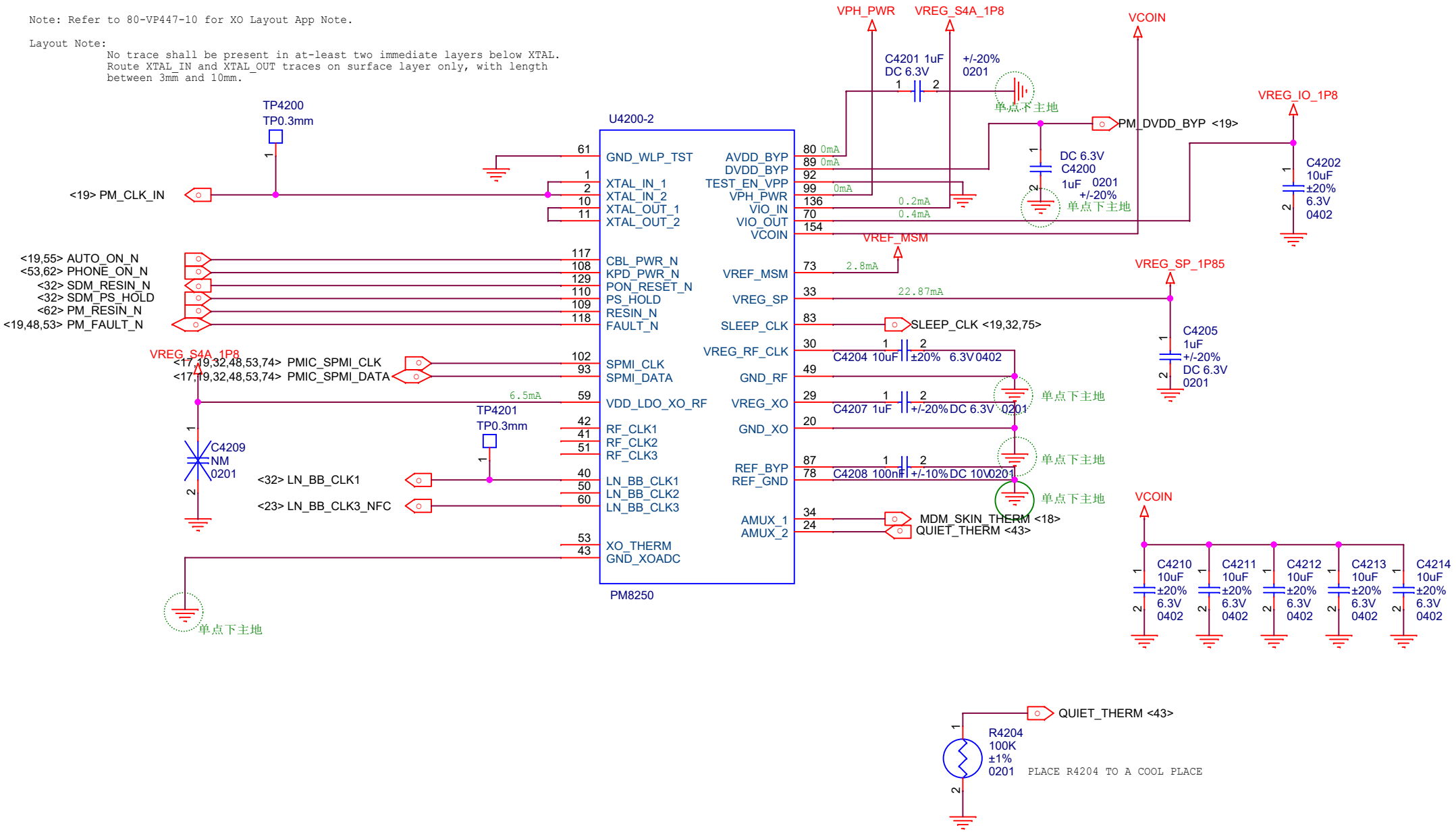
Title	J11 MAIN
Size: A4	Document Number: SDM855 PWR4
Date: Monday, December 23, 2019	Sheet 41 74



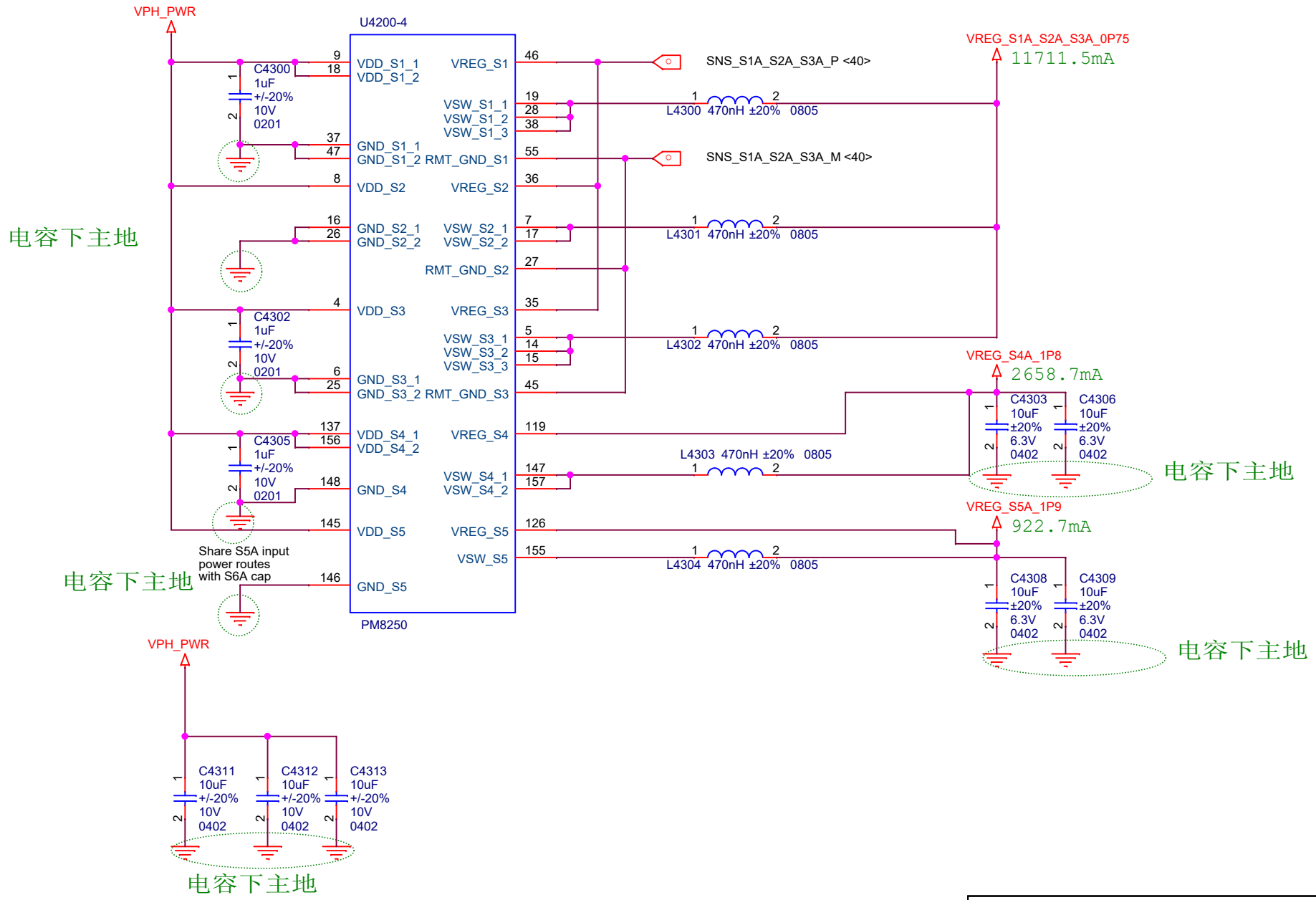
Title	J11 MAIN	
Size A3	Document Number SDM855 GND	
Date: Monday, December 23, 2019	Sheet	

Note: Refer to 80-VP447-10 for XO Layout App Note.

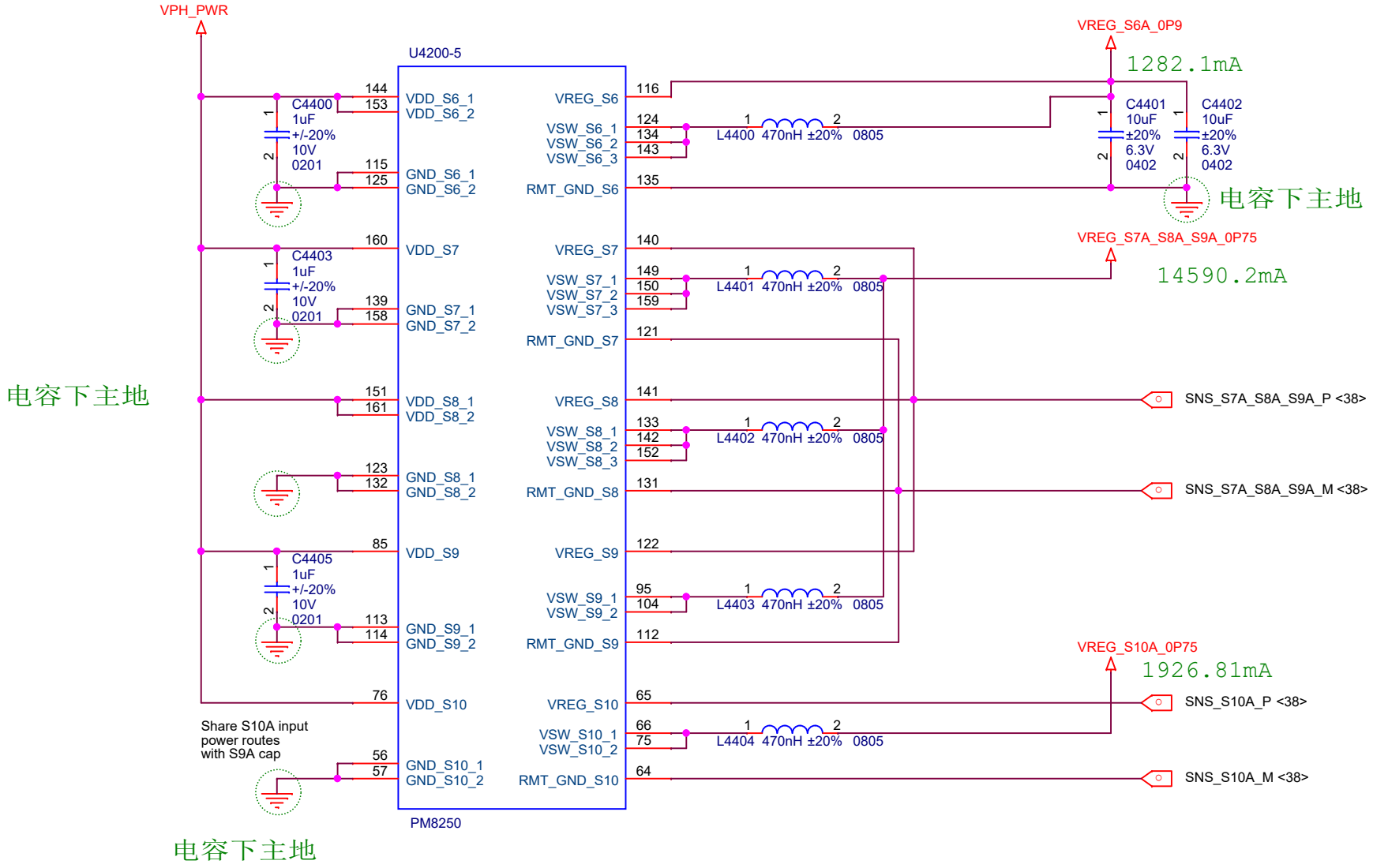
Layout Note:
No trace shall be present in at-least two immediate layers below XTAL.
Route XTAL_IN and XTAL_OUT traces on surface layer only, with length between 3mm and 10mm.



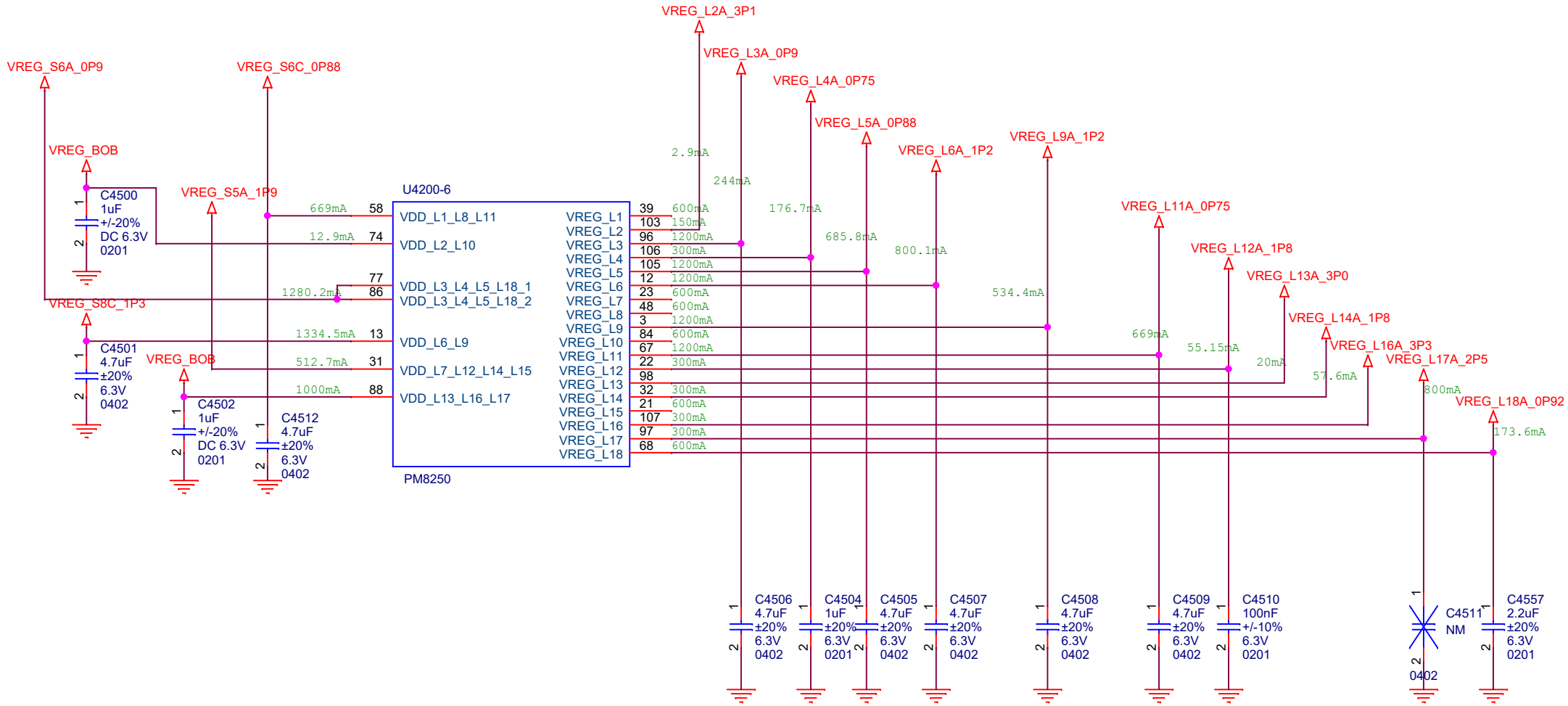
Title	J11 MAIN	
Size A4	Document Number PM855 XO&CTRL	
Date: Monday, December 23, 2019	Sheet 43 of 74	



Title	J11 MAIN	
Size A4	Document Number PM855 BUCK CONVERTER1	
Date: Monday, December 23, 2019	Sheet 44 of	

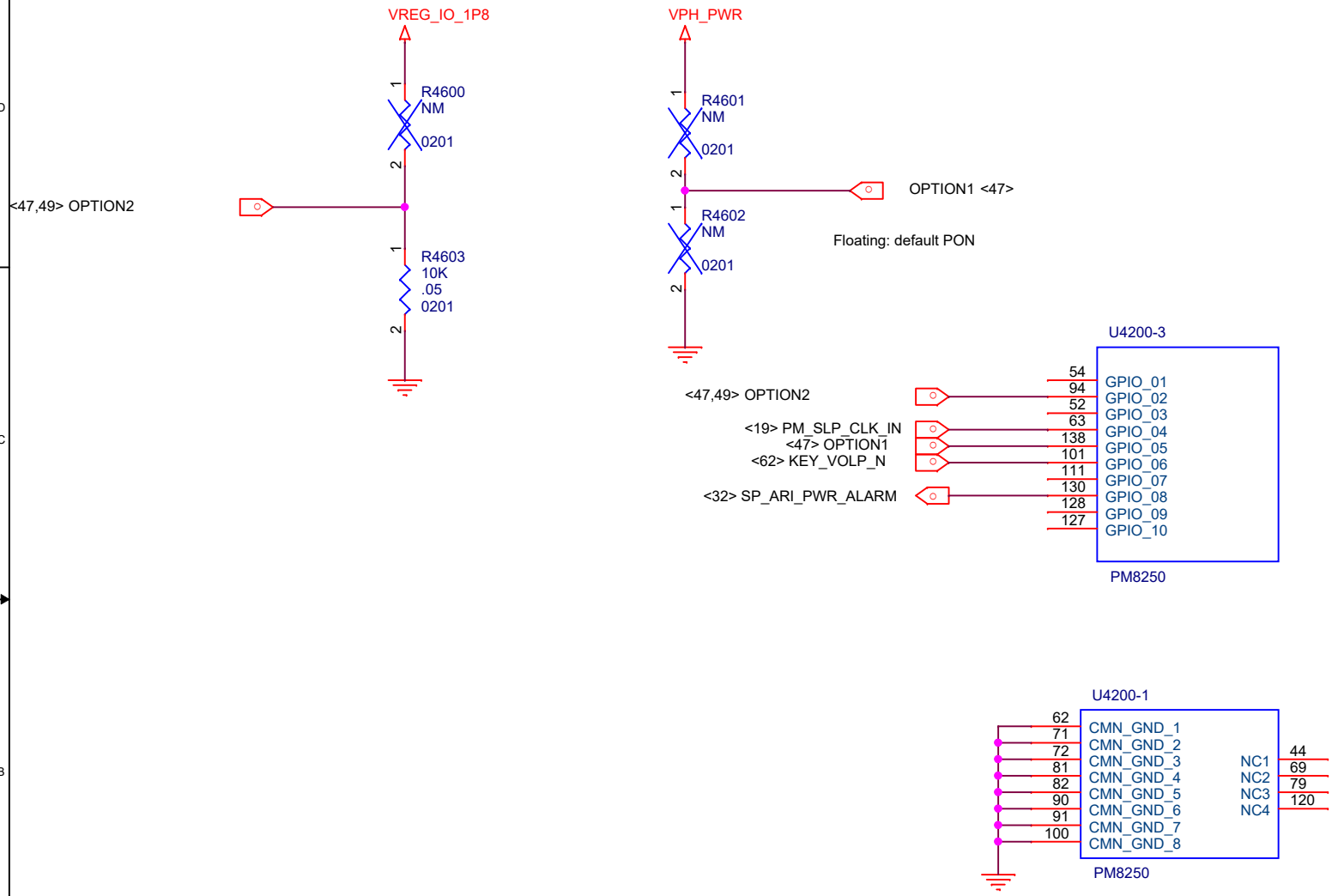


Title	J11 MAIN	
Size A4	Document Number PM855 BUCK CONVERTER2	P0
Date: Monday, December 23, 2019	Sheet 45 of 74	

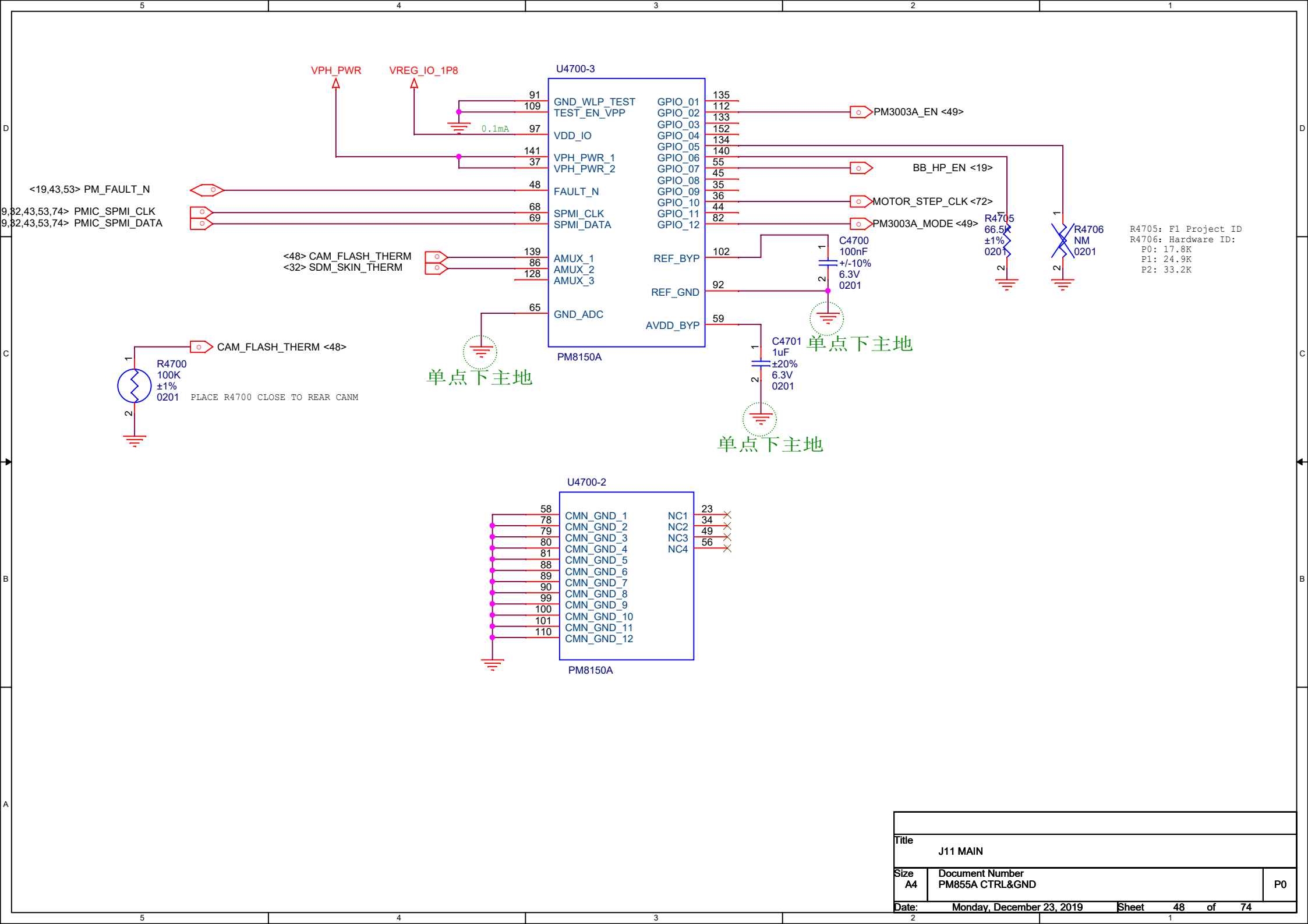


Pseudo capless allows users to place the LDO output capacitor physically/electrically far from the LDO output, near the load. The routing ESL/ESR between the PMIC pin and the remote Cout should meet the capless LDO spec.
All PMOS LDOs are considered pseudo-capless, unless it has internal PMIC load. If an internal PMIC load, the output cap must be placed close to the PMIC.
Required capacitance for each LDO type can be found in App Note: 80-VT310-125

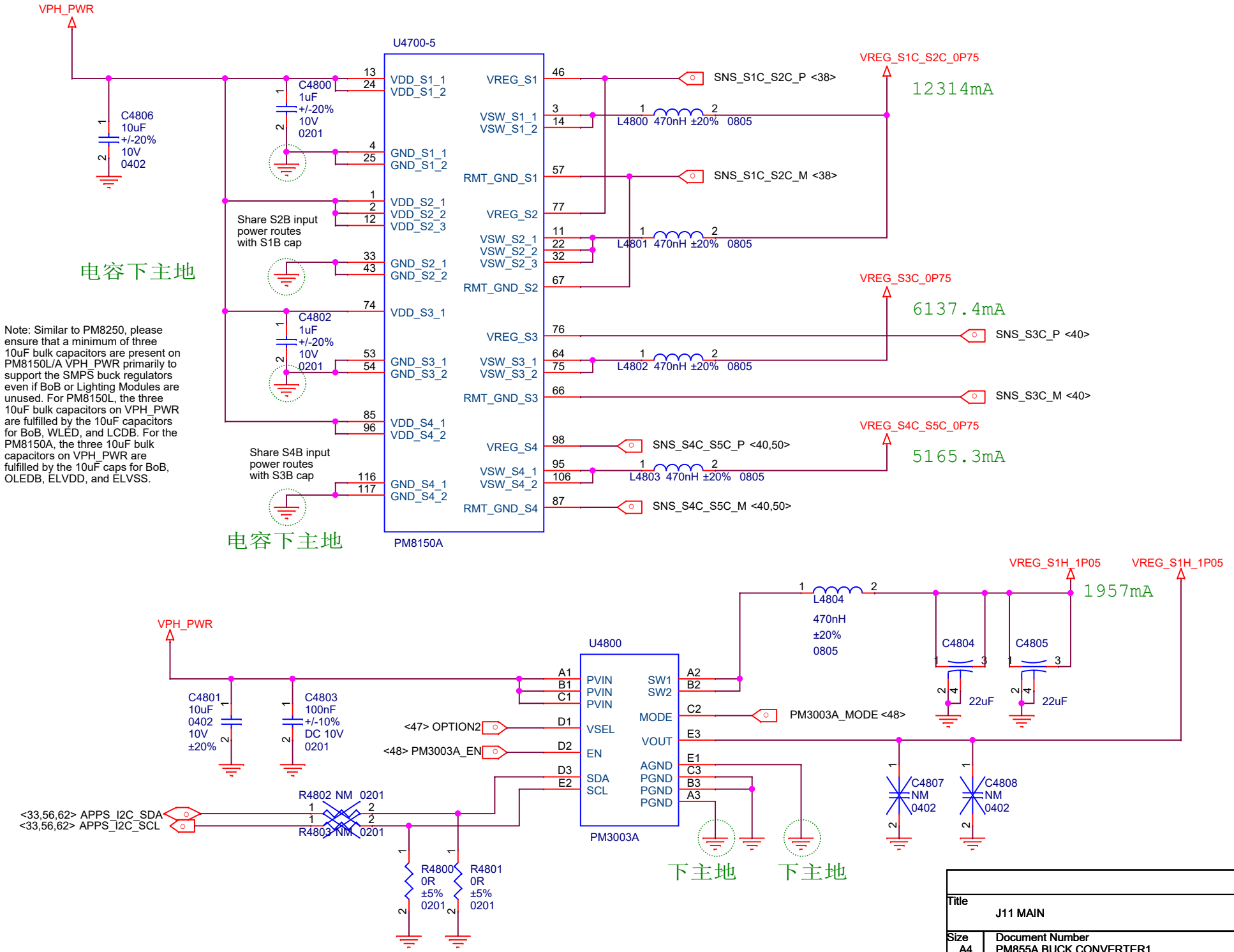
Title	J11 MAIN	
Size A4	Document Number PM855 LDOs	
Date: Monday, December 23, 2019	Sheet 46 of 74	



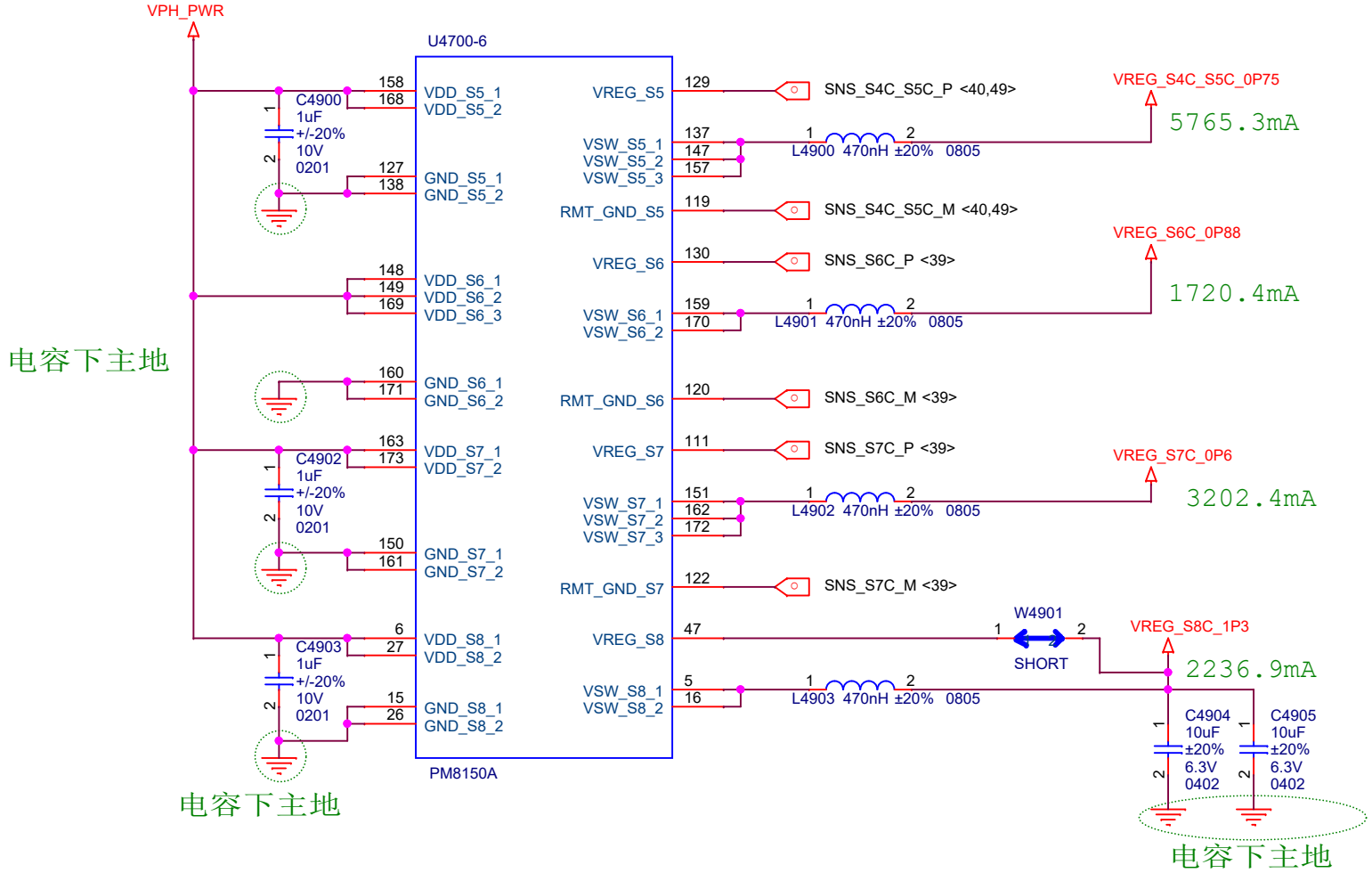
Title	J11 MAIN	
Size A4	Document Number PM855 GPIO&GND	
Date: Monday, December 23, 2019	Sheet	



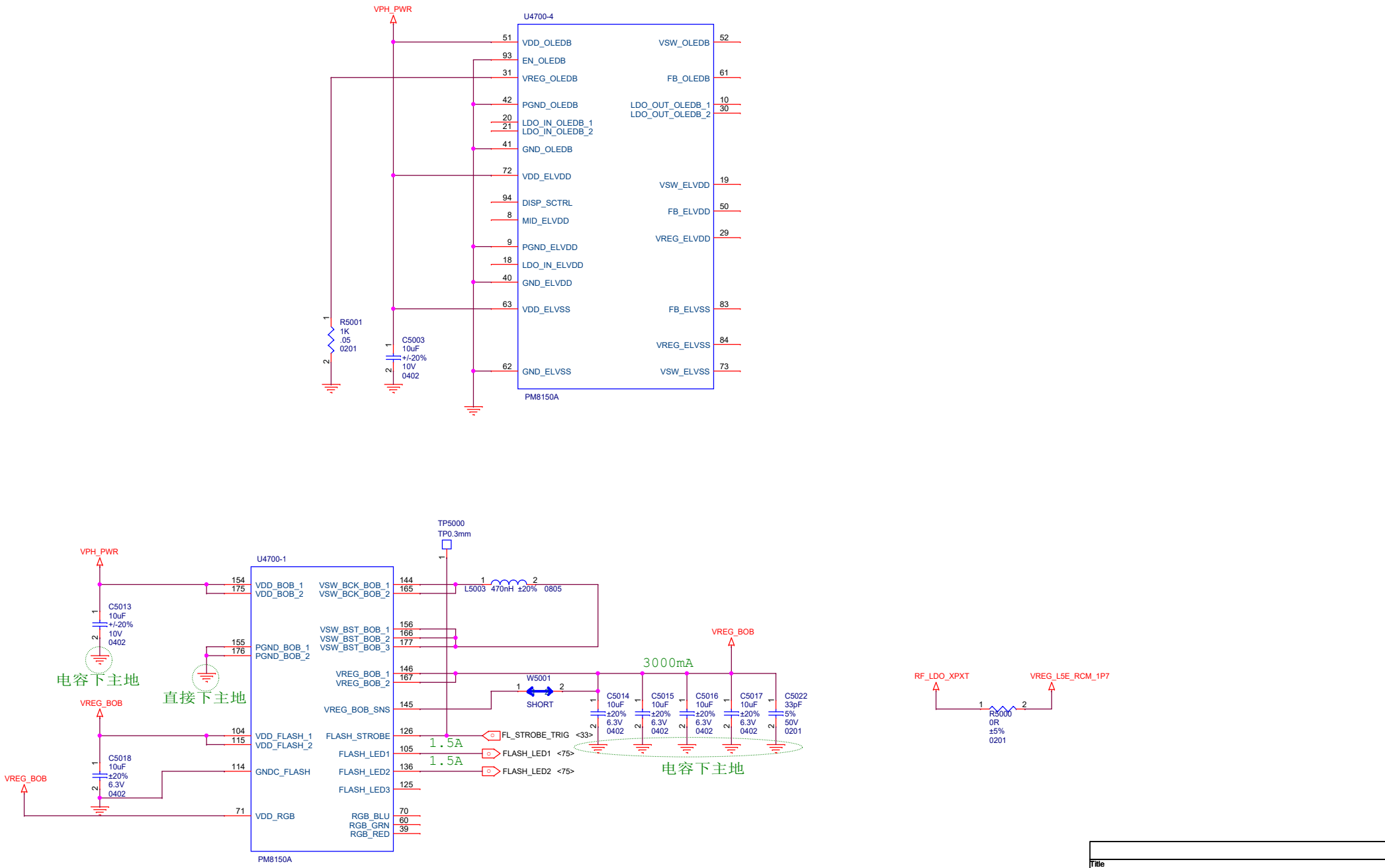
Title	J11 MAIN	
Size A4	Document Number PM855A CTRL&GND	P0
Date: Monday, December 23, 2019	Sheet 48 of 74	



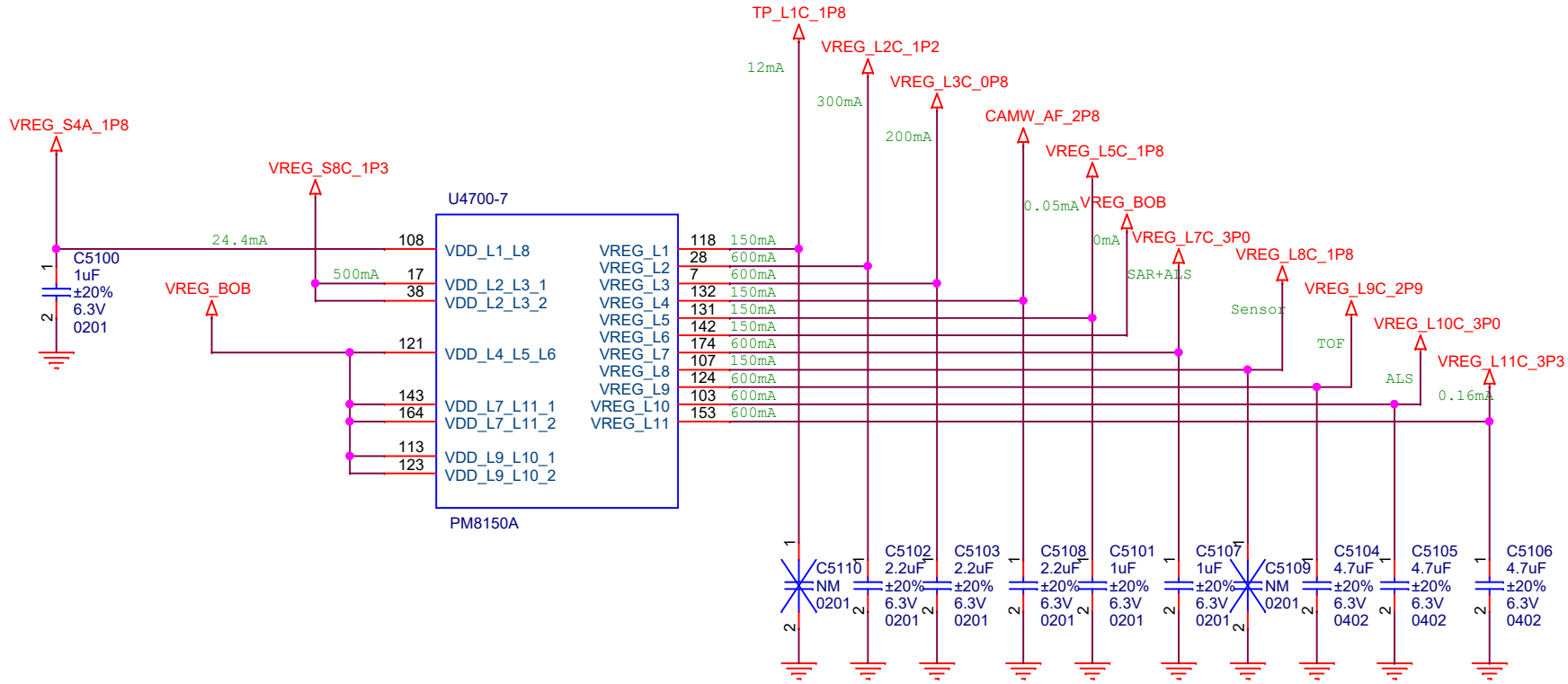
Title	J11 MAIN	
Size A4	Document Number PM855A BUCK CONVERTER1	
Date: Monday, December 23, 2019	Sheet 49 of 74	



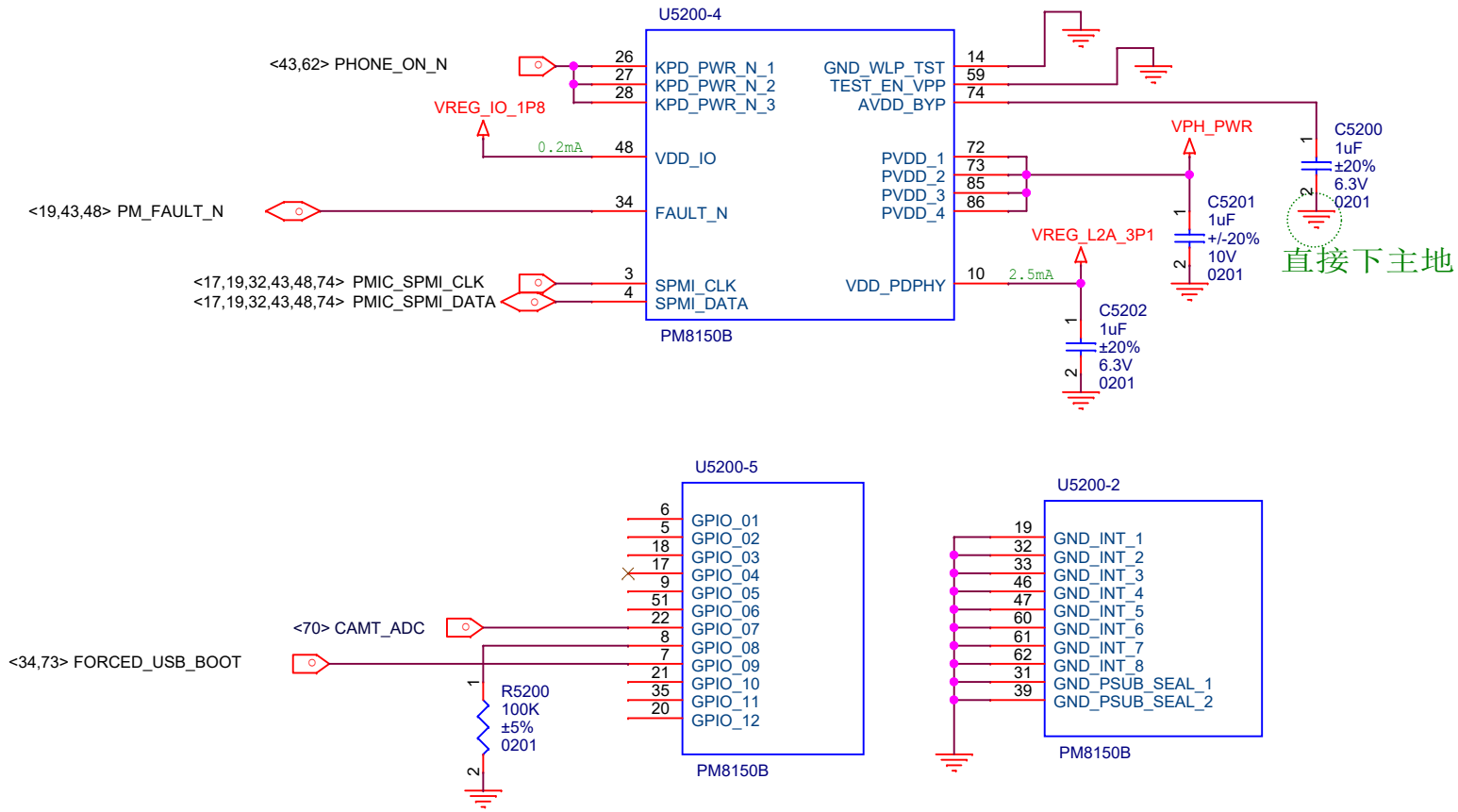
Title	J11 MAIN	
Size A4	Document Number PM855A BUCK CONVERTER2	P0
Date: Monday, December 23, 2019	Sheet 50 of 74	



Title	J11 MAIN	
Size A3	Document Number PM855A AMOLED&BOB&FLASH	
Date: Monday, December 23, 2019	Sheet 51 of 74	

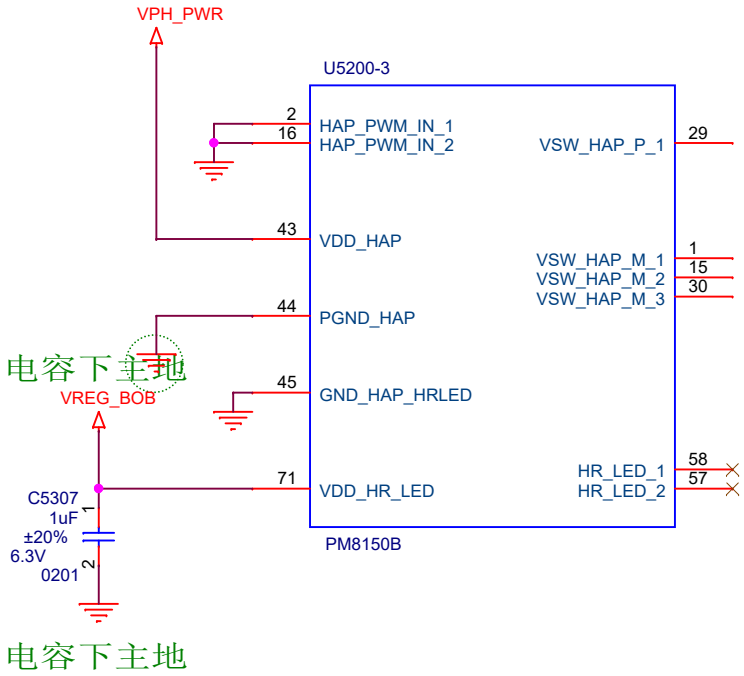


Title	J11 MAIN	
Size A4	Document Number PM855A LDOs	
Date: Monday, December 23, 2019	Sheet 52 of 74	



Note: GPIO_04 and GPIO_11 of PM8150B are for internal usage. Keep them float.
Keep GPIO_03 of PM8150B float. Don't use it for other purpose.
GPIO_06 of PM8150B is dedicated for SMB_STAT. Don't use it for other purpose.

Title	J11 MAIN	
Size A4	Document Number PM855B CTRL&GND	
Date: Monday, December 23, 2019	Sheet 53 of 74	



Title	J11 MAIN	
Size A4	Document Number PM855B HAPTIC	
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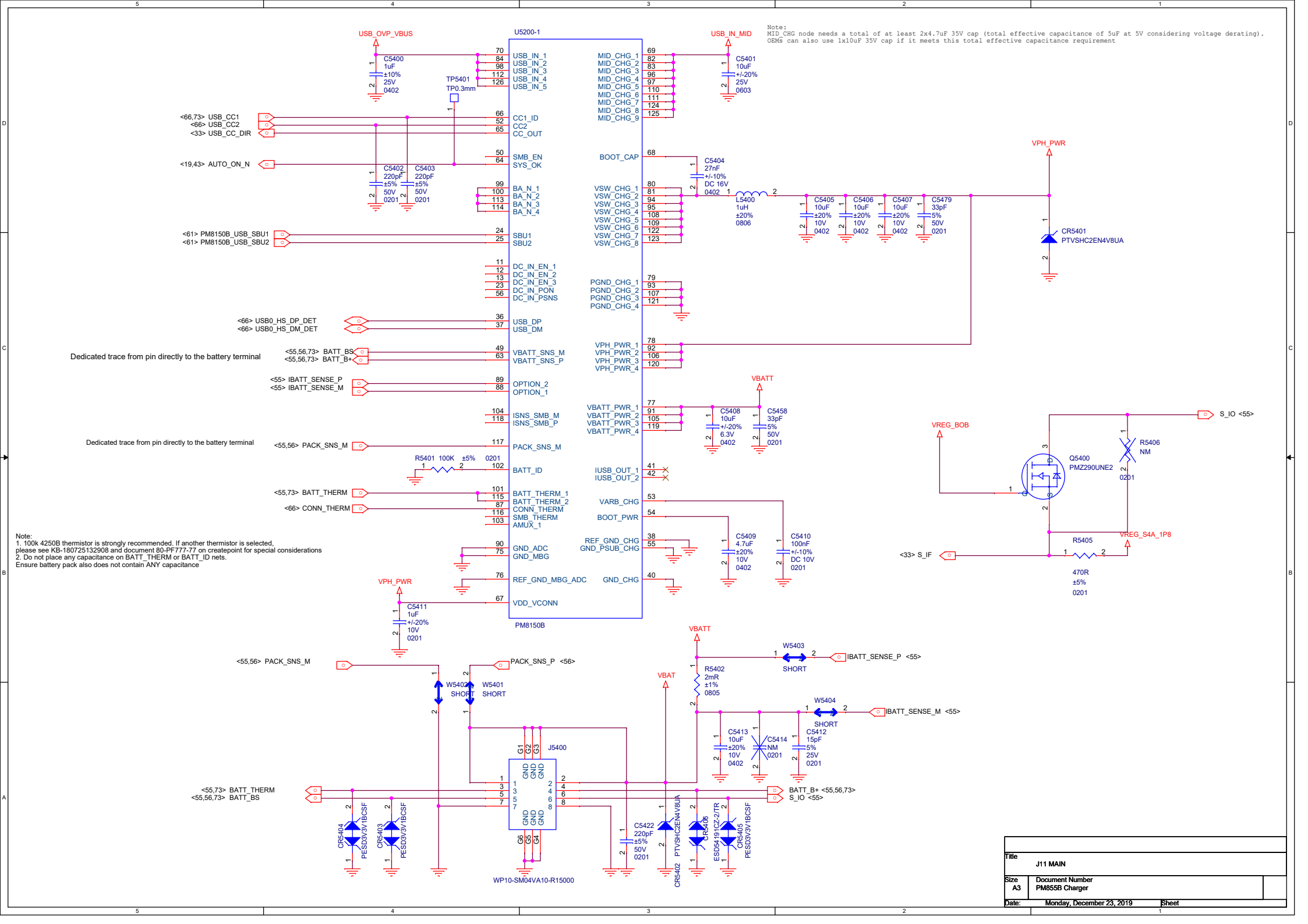
Note:
MID_CHG node needs a total of at least 2x4.7uF 35V cap (total effective capacitance of 5uF at 5V considering voltage derating).
OEMs can also use 1x10uF 35V cap if it meets this total effective capacitance requirement
U5200-1
PM8150B
USB_OVP_VBUS
USB_IN_MID
VPH_PWR
VBATT
VBAT
VREG_BOB
VREG_S4A_1P8
Dedicated trace from pin directly to the battery terminal
Dedicated trace from pin directly to the battery terminal
Note:
1. 100k 4250B thermistor is strongly recommended. If another thermistor is selected,
please see KB-180725132908 and document 80-PF777-77 on createpoint for special considerations
2. Do not place any capacitance on BATT_THERM or BATT_ID nets.
Ensure battery pack also does not contain ANY capacitance
WP10-SM04VA10-R15000
Title
J11 MAIN
Size
A3
Document Number
PM855B Charger
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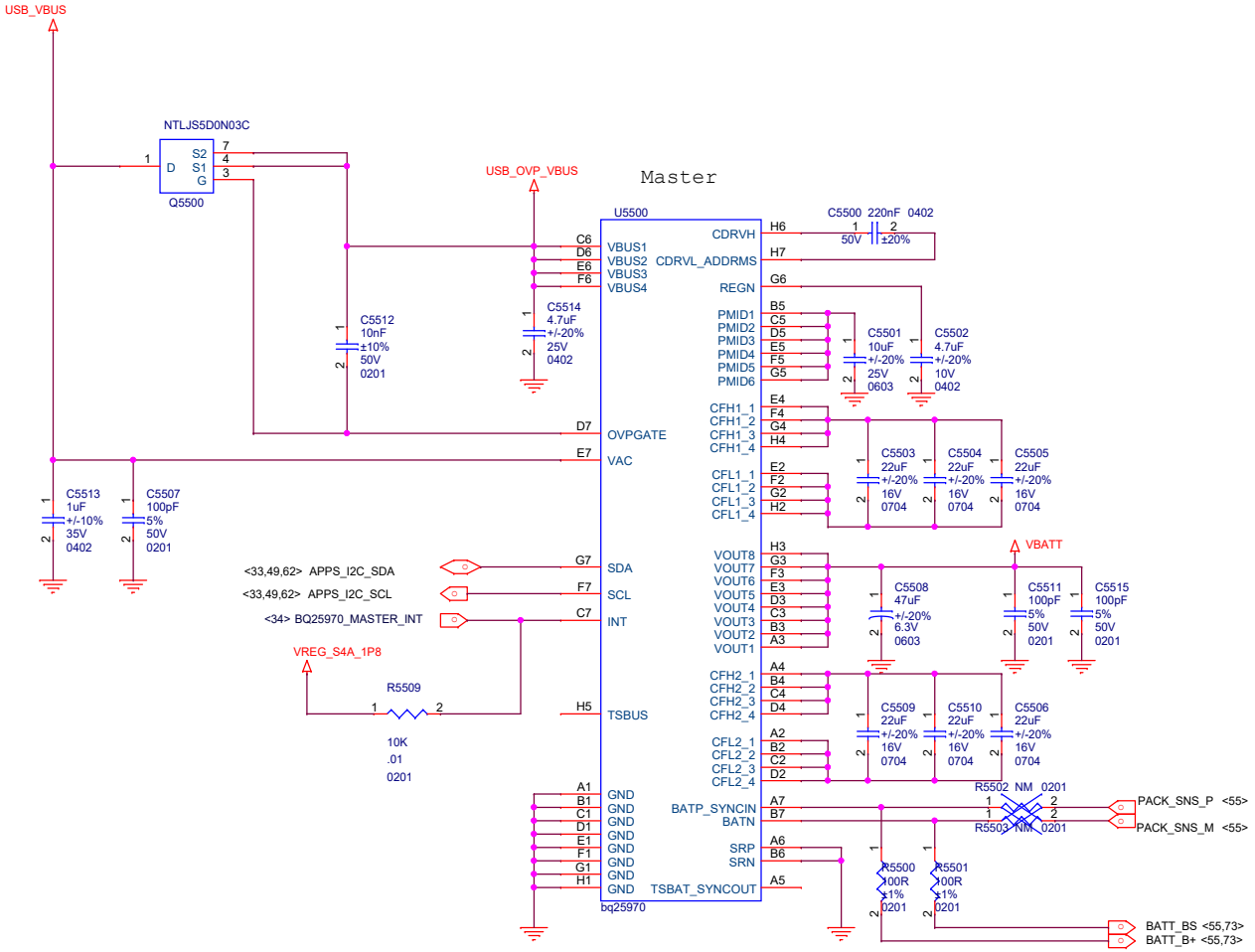
Sheet



Title	F1 MAIN	
Size A3	Document Number SMB1390&WL POWER	
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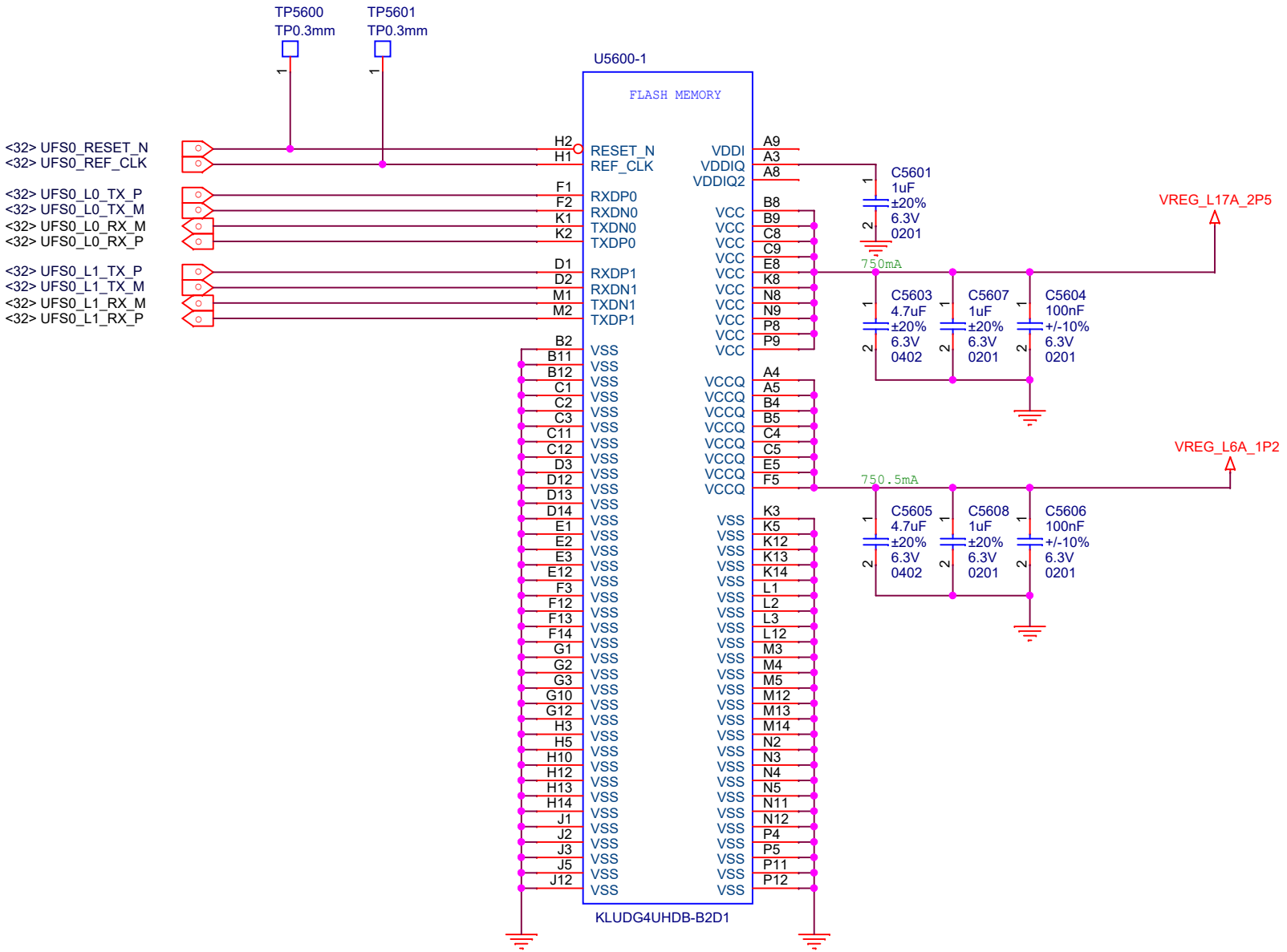

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Size A4	Document Number MEMORY	
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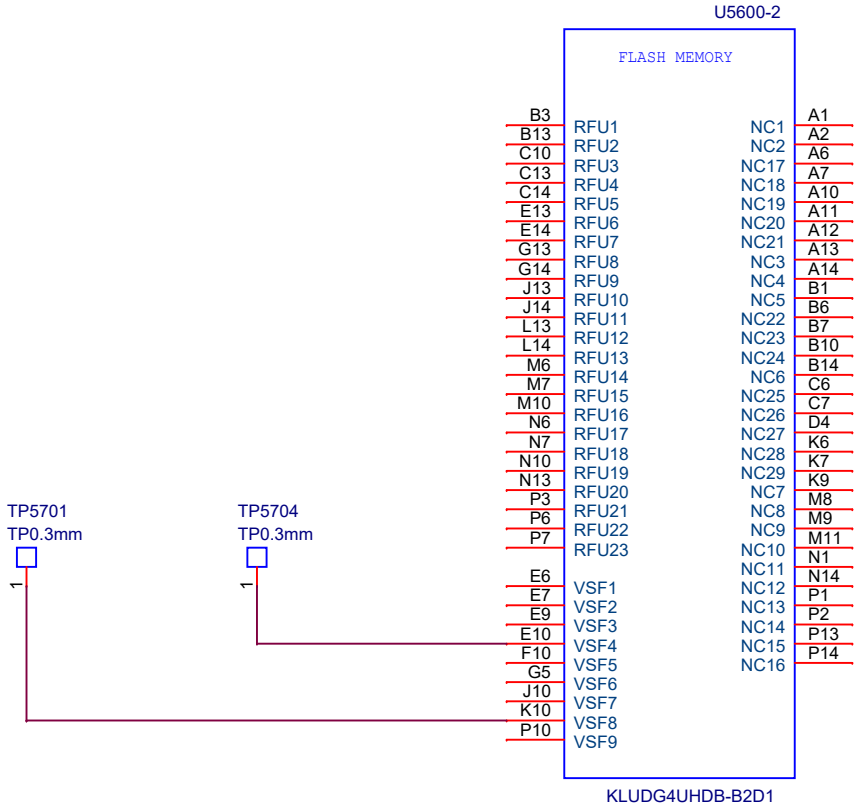

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Size A4	Document Number MEMORY-2	
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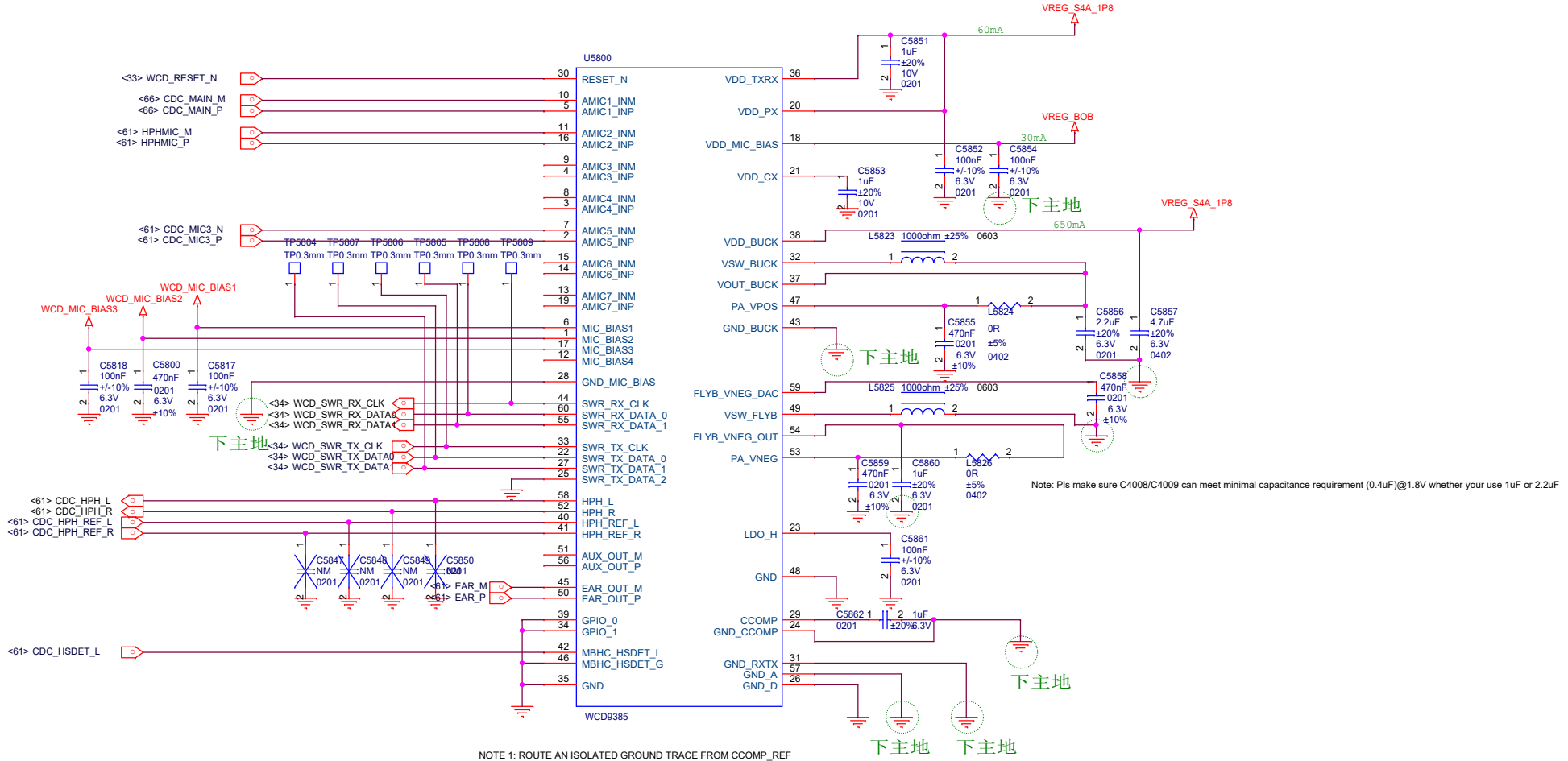

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Size A3	Document Number WCD9340-1	
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Title	J11 MAIN
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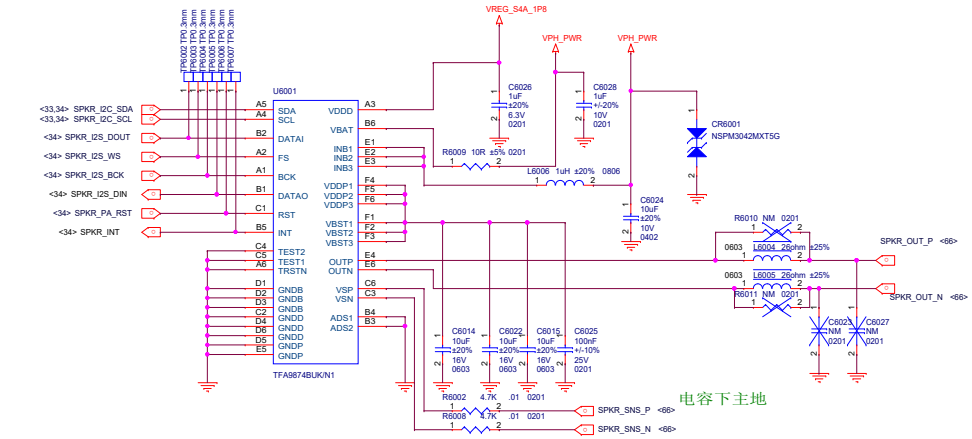
SPKR PA



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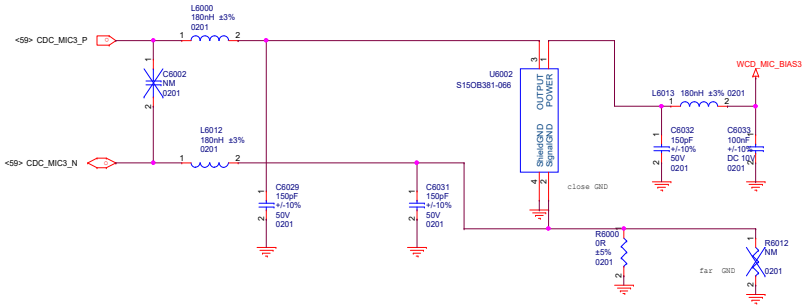
AUX MIC



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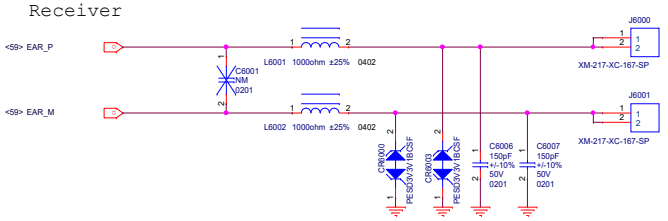

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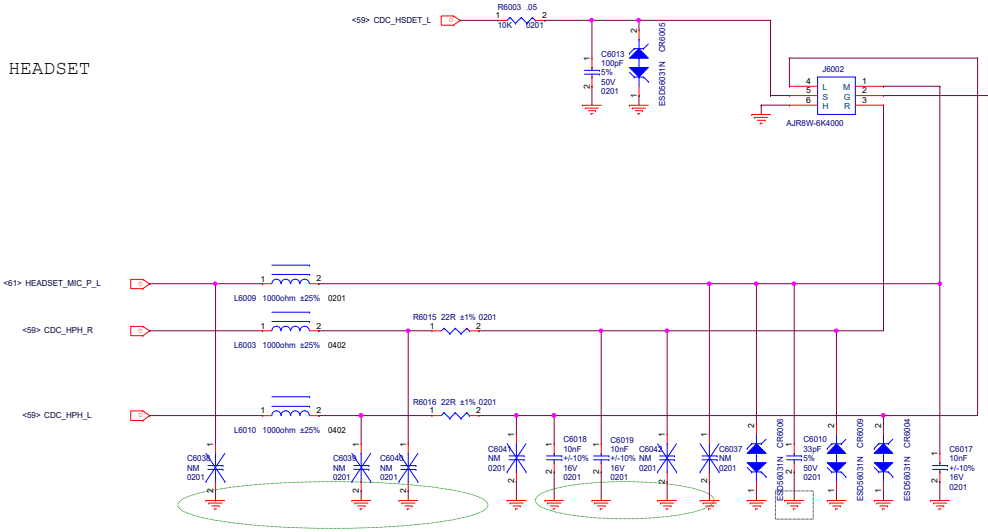

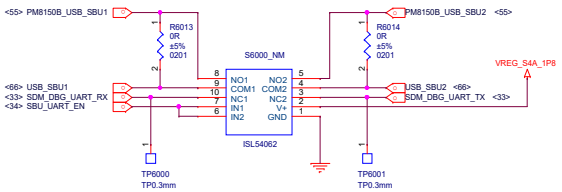

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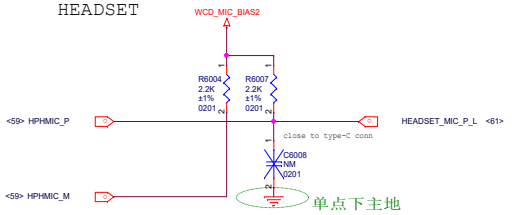

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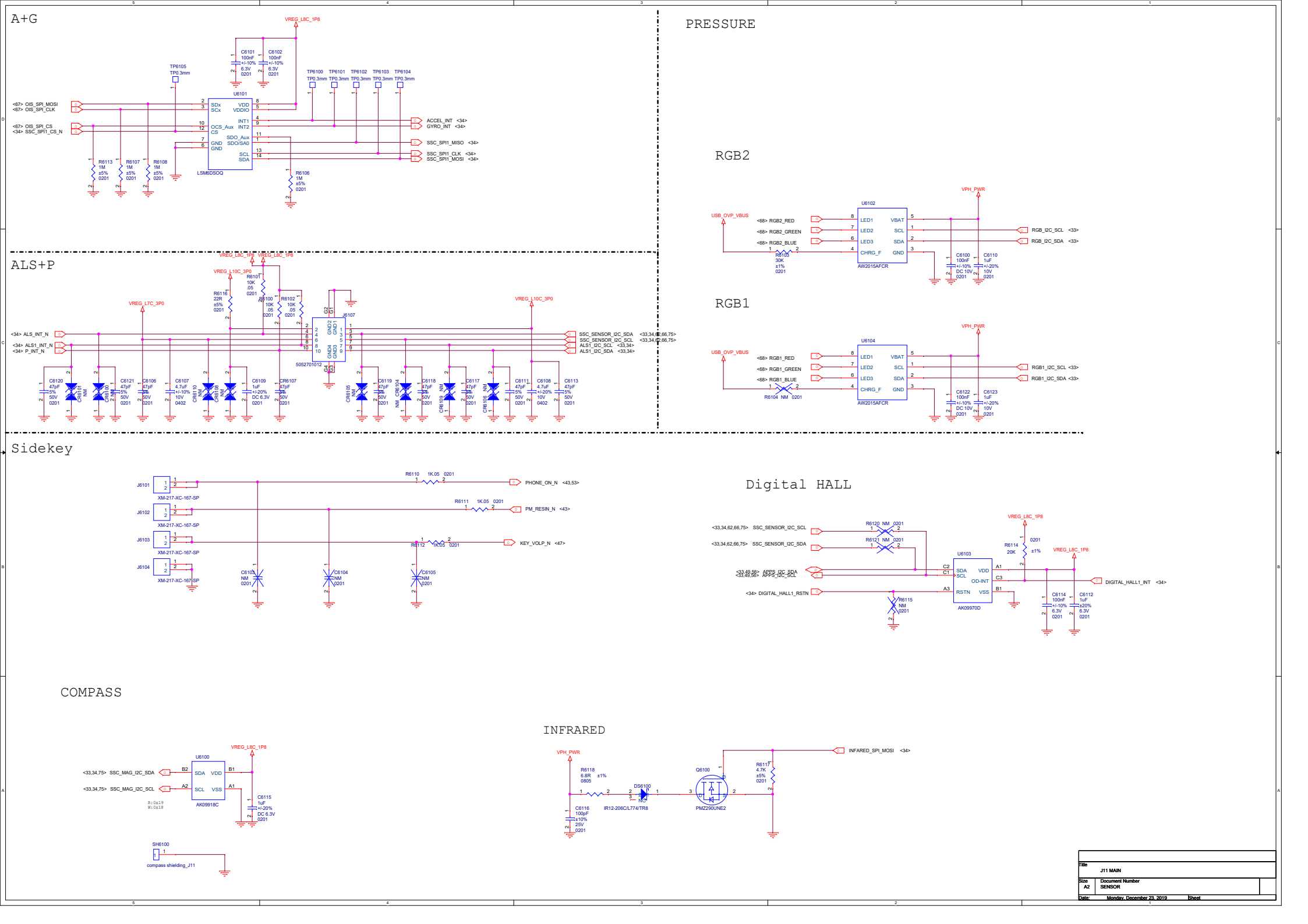
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PRESSURE
RGB2
RGB1
ALS+P
Sidekey
Digital HALL
COMPASS
INFRARED
U6101
LSM6DSOQ
U6102
AW2015AFCR
U6104
AW2015AFCR
U6103
AK09970D
U6100
AK09918C
Q6100
PMZ290UNE2
J6101
J6102
J6103
J6104
J6107
SH6100
compass shielding_J11
VREG_L8C_1P8
VREG_L10C_3P0
VREG_L7C_3P0
VPH_PWR
USB_OVP_VBUS
PHONE_ON_N <43,53>
PM_RESIN_N <43>
KEY_VOLP_N <47>
DIGITAL_HALL1_INT <34>
INFARED_SPI_MOSI <34>
RGB_I2C_SCL <33>
RGB_I2C_SDA <33>
RGB1_I2C_SCL <33>
RGB1_I2C_SDA <33>
ACCEL_INT <34>
GYRO_INT <34>
SSC_SPI1_MISO <34>
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Title
J11 MAIN
Size
A2
Document Number
SENSOR
Date:
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Sheet

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FLASH

TOF

COMPASS

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Size: A4	Document Number: SIM
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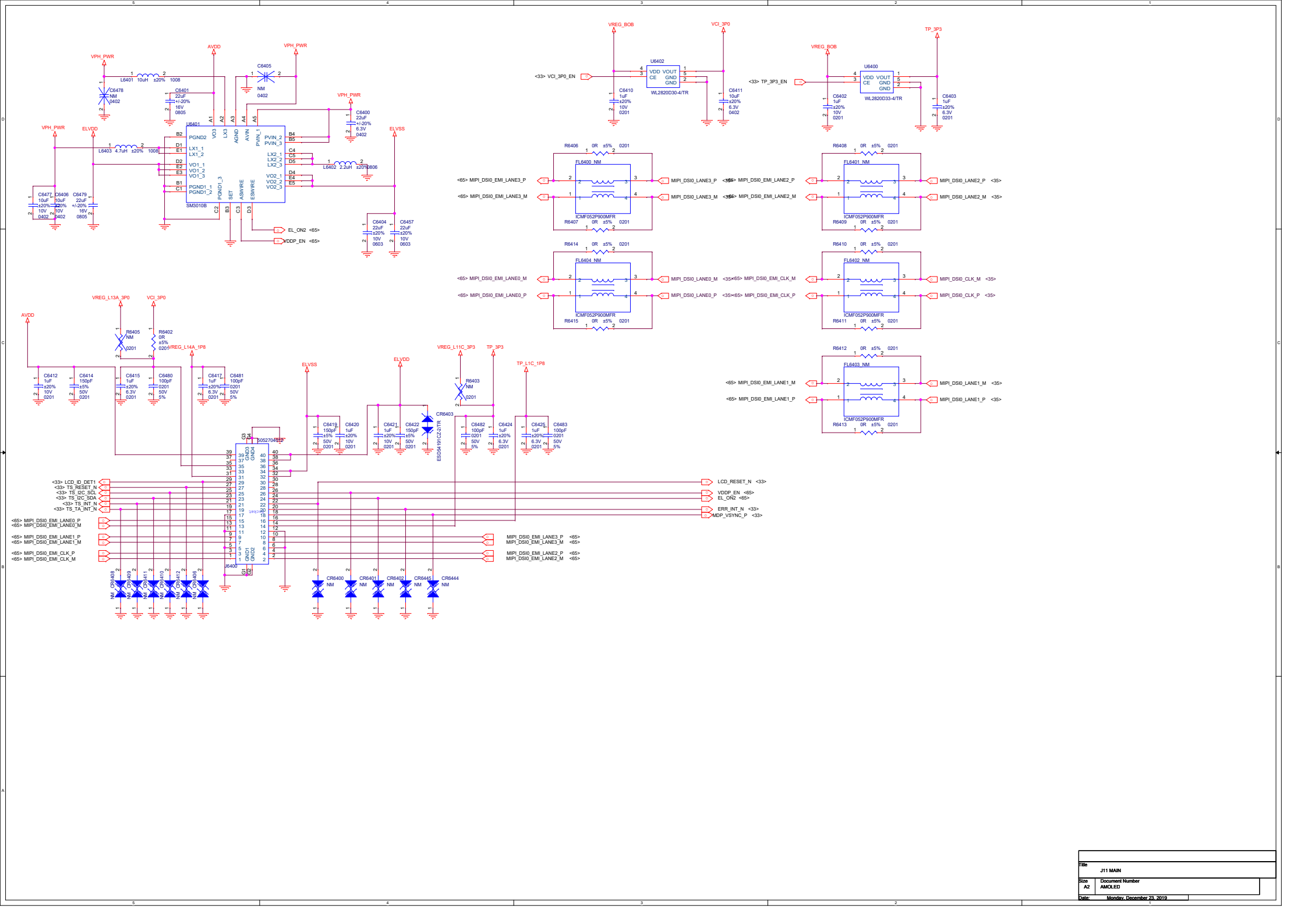

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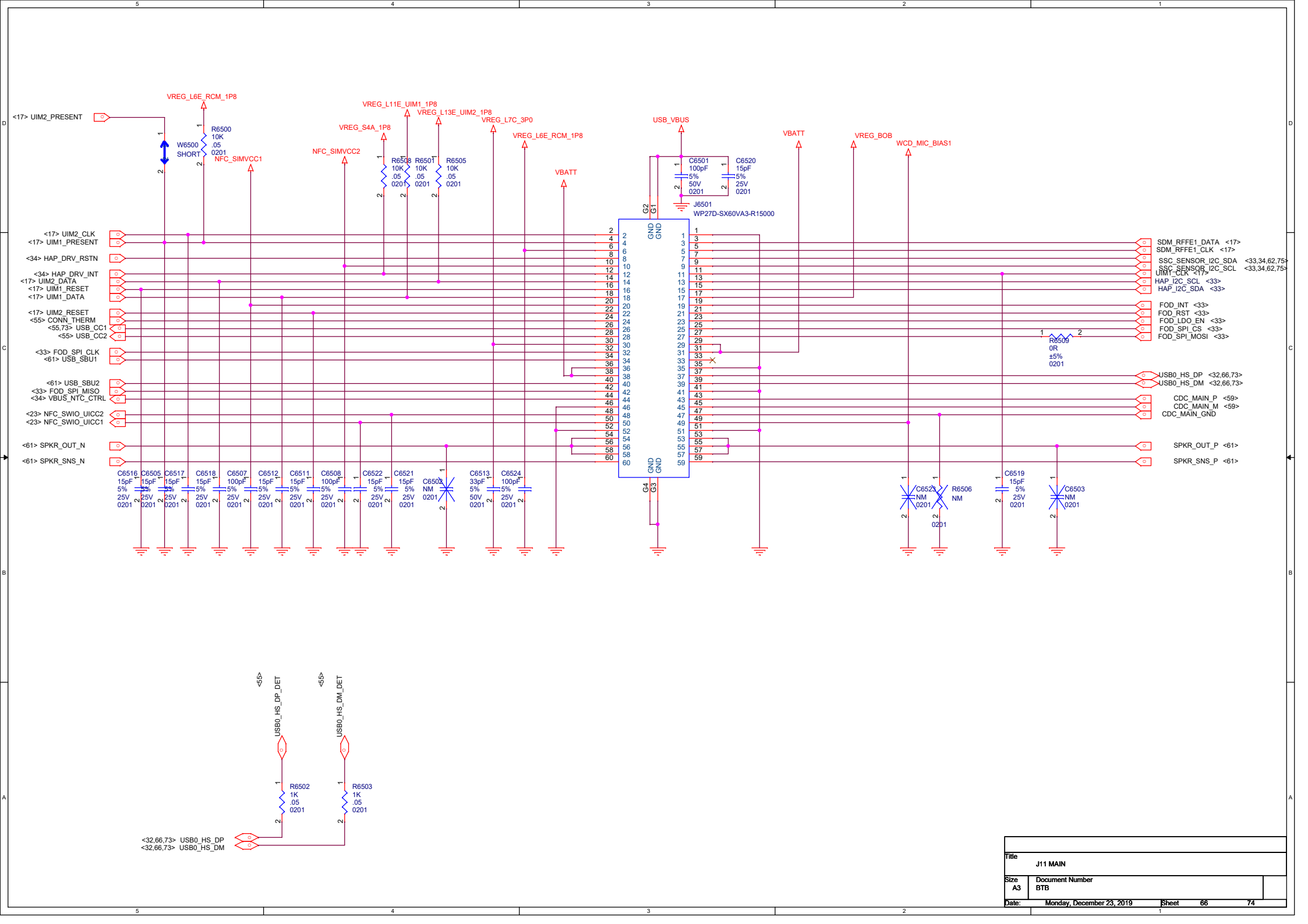
Document Number	AMOLED
Date:	Monday, December 23, 2019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W6500 SHORT
NFC_SIMVCC1
VREG_L11E_UIM1_1P8
VREG_L13E_UIM2_1P8
VREG_S4A_1P8
VREG_L7C_3P0
VREG_L6E_RCM_1P8
NFC_SIMVCC2
R6508 10K .05 0201
R6501 10K .05 0201
R6505 10K .05 0201
VBATT
USB_VBUS
C6501 100pF 5% 50V 0201
C6520 15pF 5% 25V 0201
J6501
WP27D-SX60VA3-R15000
VBATT
VREG_BOB
WCD_MIC_BIAS1
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<55> CONN_THERM
<55,73> USB_CC1
<55> USB_CC2
<33> FOD_SPI_CLK
<61> USB_SBU1
<61> USB_SBU2
<33> FOD_SPI_MISO
<34> VBUS_NTC_CTRL
<23> NFC_SWIO_UICC2
<23> NFC_SWIO_UICC1
<61> SPKR_OUT_N
<61> SPKR_SNS_N
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SDM_RFFE1_CLK <17>
SSC_SENSOR_I2C_SDA <33,34,62,75>
SSC_SENSOR_I2C_SCL <33,34,62,75>
UIM1_CLK <17>
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HAP_I2C_SDA <33>
FOD_INT <33>
FOD_RST <33>
FOD_LDO_EN <33>
FOD_SPI_CS <33>
FOD_SPI_MOSI <33>
R6509 0R ±5% 0201
USB0_HS_DP <32,66,73>
USB0_HS_DM <32,66,73>
CDC_MAIN_P <59>
CDC_MAIN_M <59>
CDC_MAIN_GND
SPKR_OUT_P <61>
SPKR_SNS_P <61>
C6516 15pF 5% 25V 0201
C6505 15pF 5% 25V 0201
C6517 15pF 5% 25V 0201
C6518 15pF 5% 25V 0201
C6507 100pF 5% 25V 0201
C6512 15pF 5% 25V 0201
C6511 15pF 5% 25V 0201
C6508 100pF 5% 25V 0201
C6522 15pF 5% 25V 0201
C6521 15pF 5% 25V 0201
C6502 NM 0201
C6513 33pF 5% 50V 0201
C6524 100pF 5% 25V 0201
C6523 NM 0201
R6506 NM 0201
C6519 15pF 5% 25V 0201
C6503 NM 0201
<55> USB0_HS_DP_DET
<55> USB0_HS_DM_DET
R6502 1K .05 0201
R6503 1K .05 0201
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J11 MAIN
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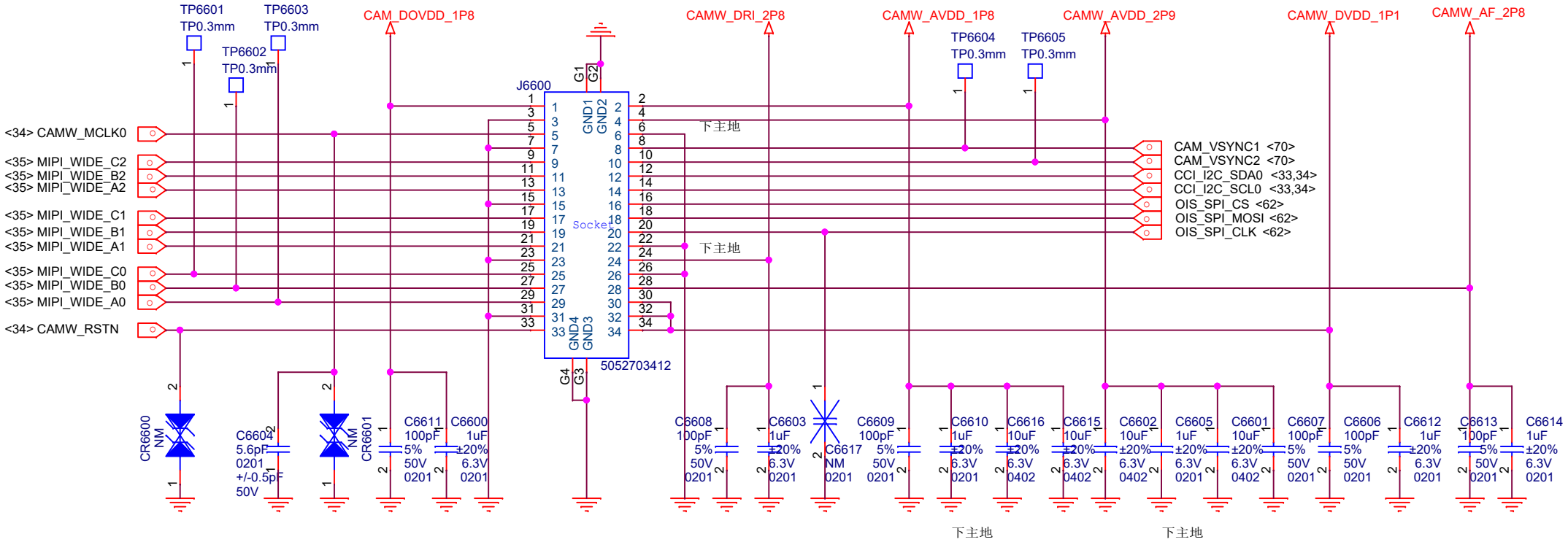
WIDE 64M



Title	J11 MAIN		
Size A4	Document Number WIDE&TELE CAMERA		
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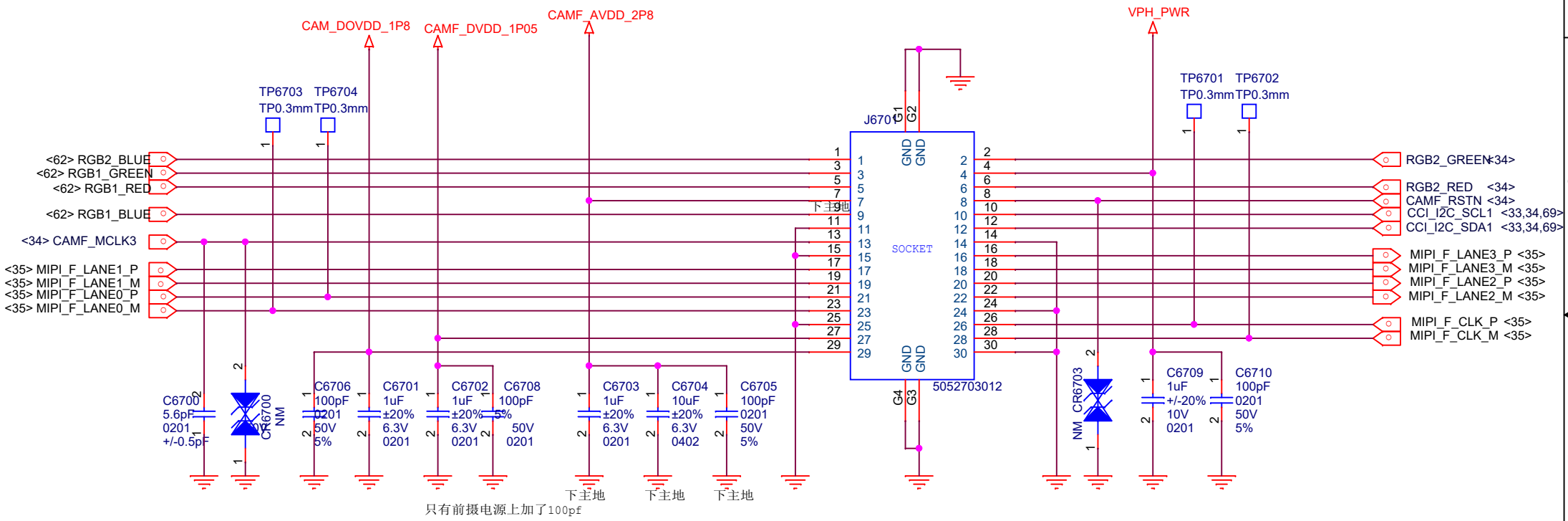

Title	J11 MAIN		
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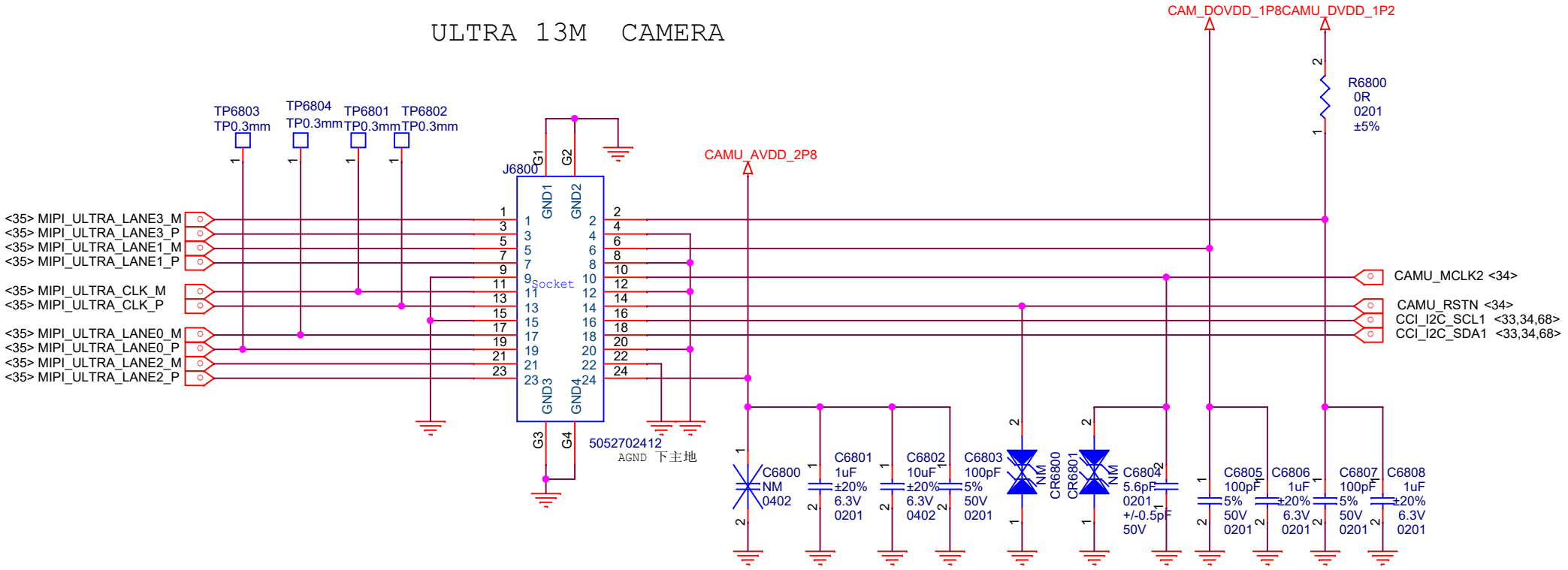
ULTRA 13M CAMERA



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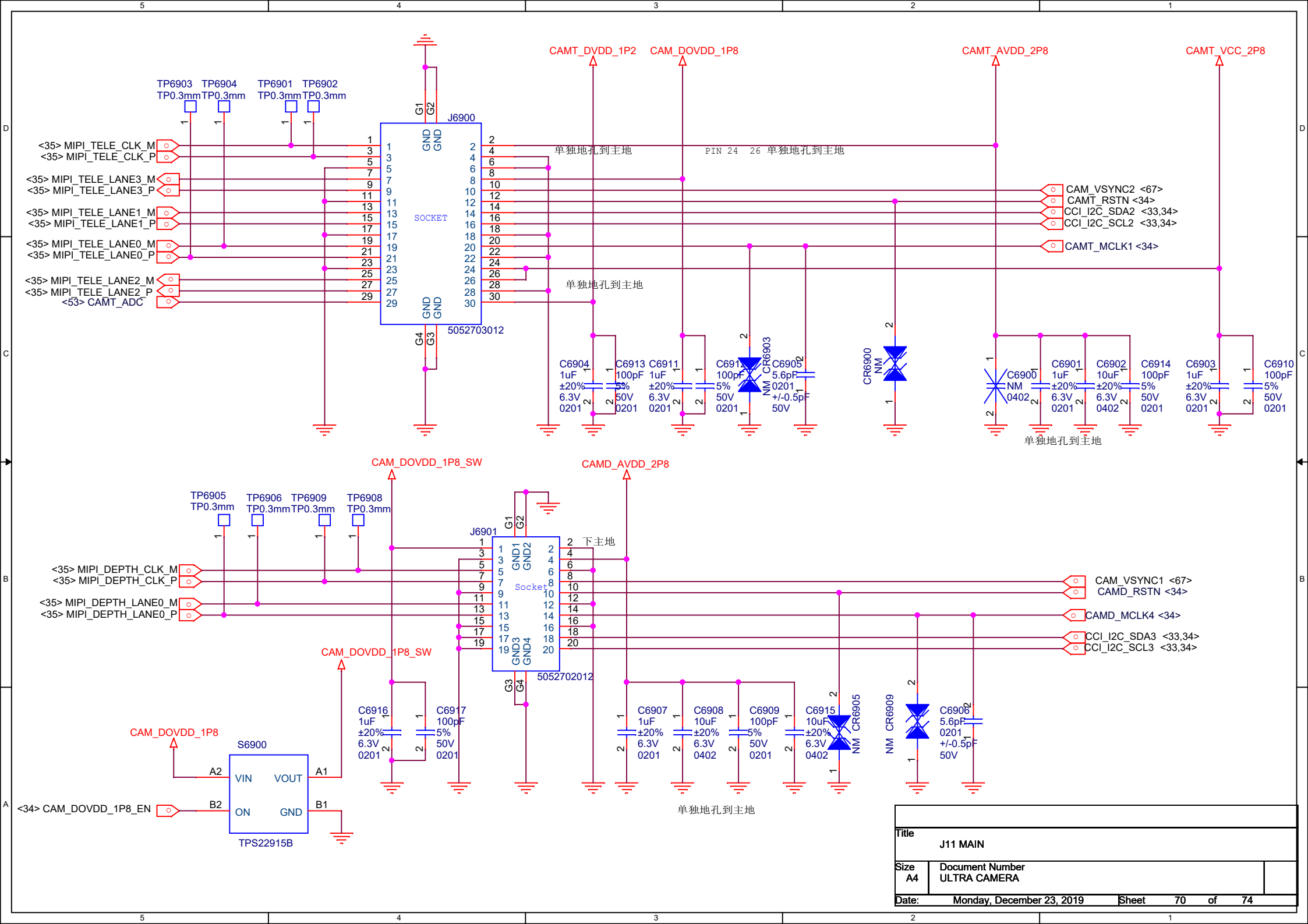

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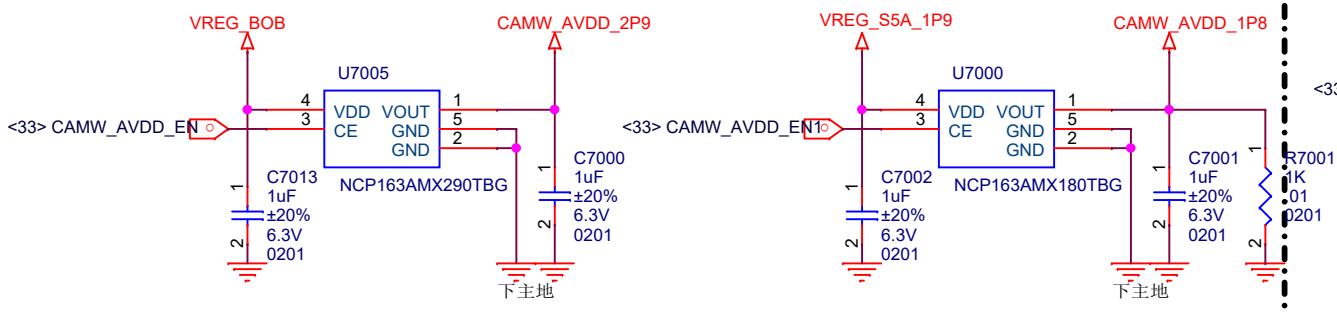
WIDE



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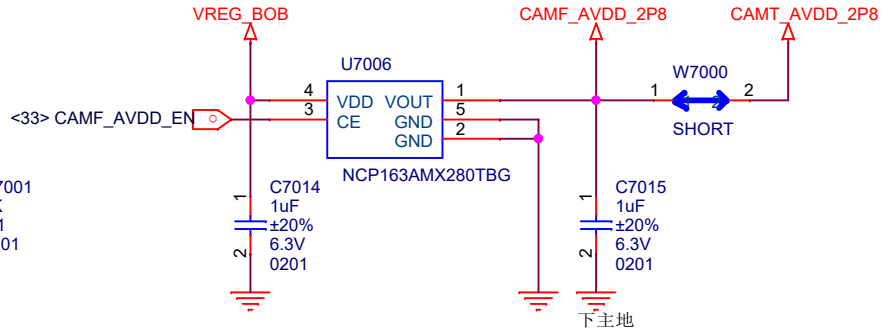
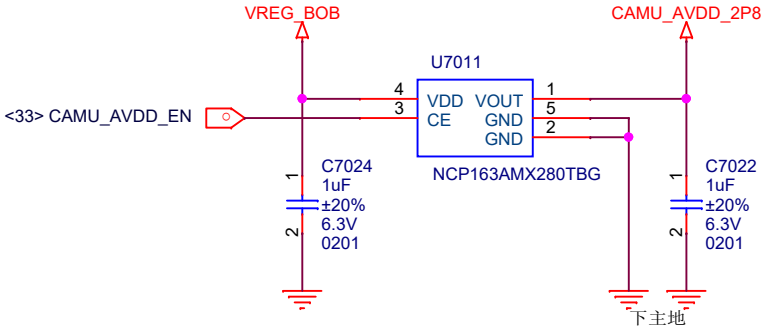


ULTRA



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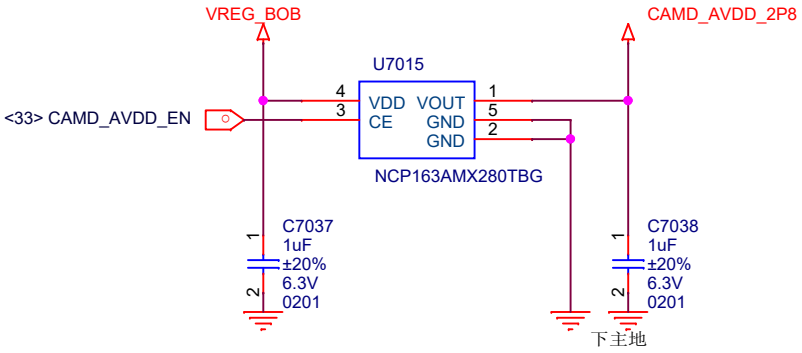

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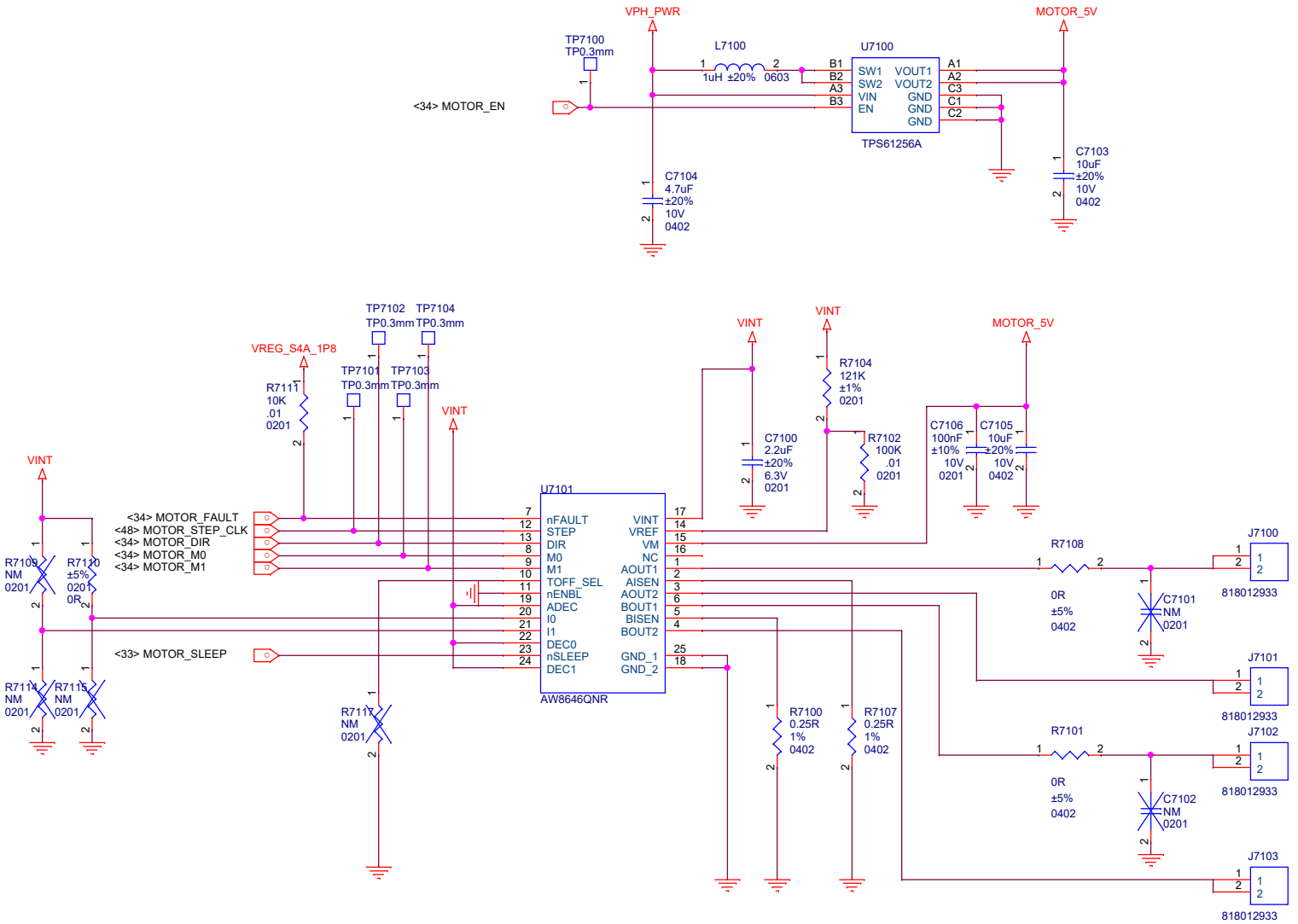

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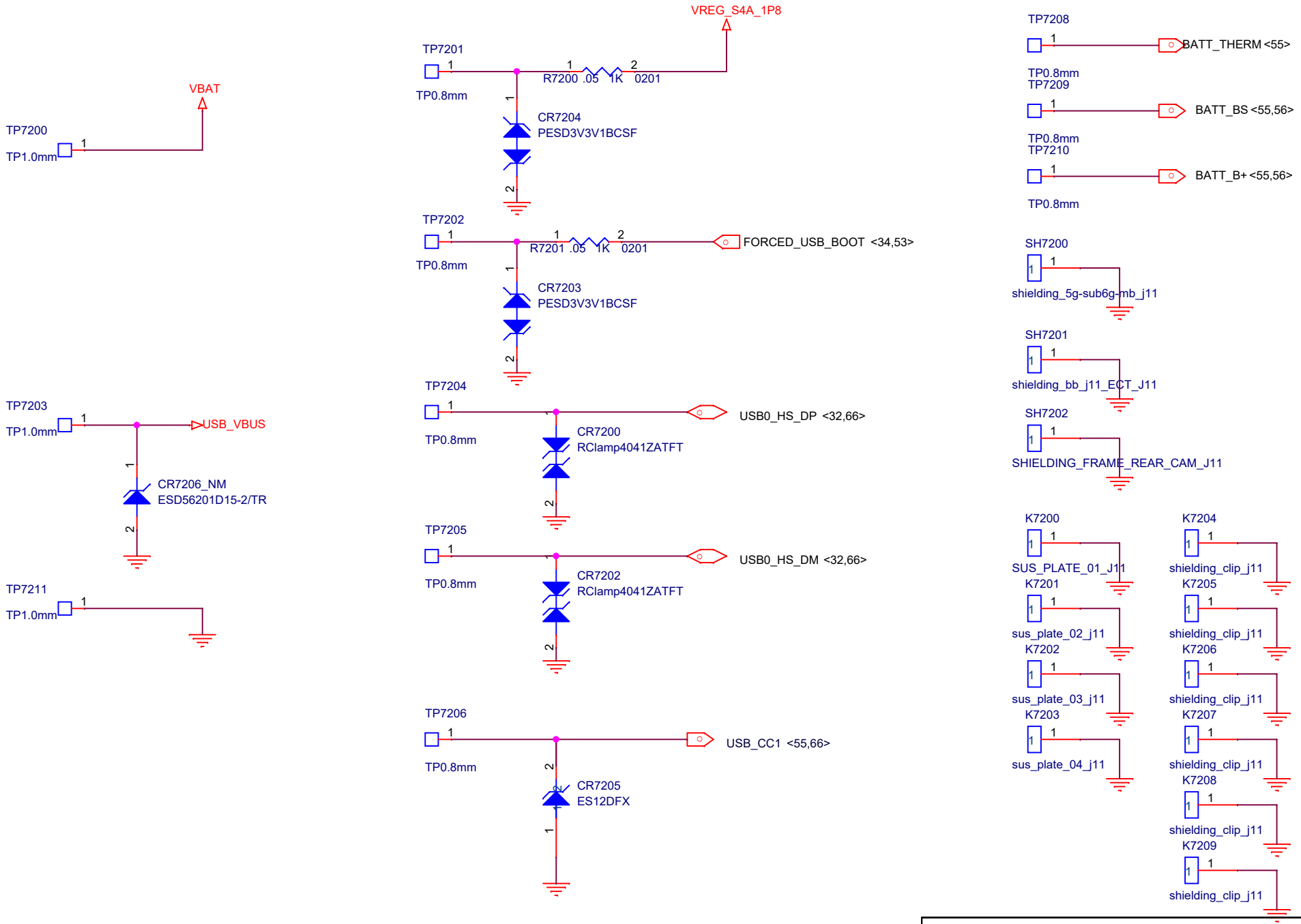

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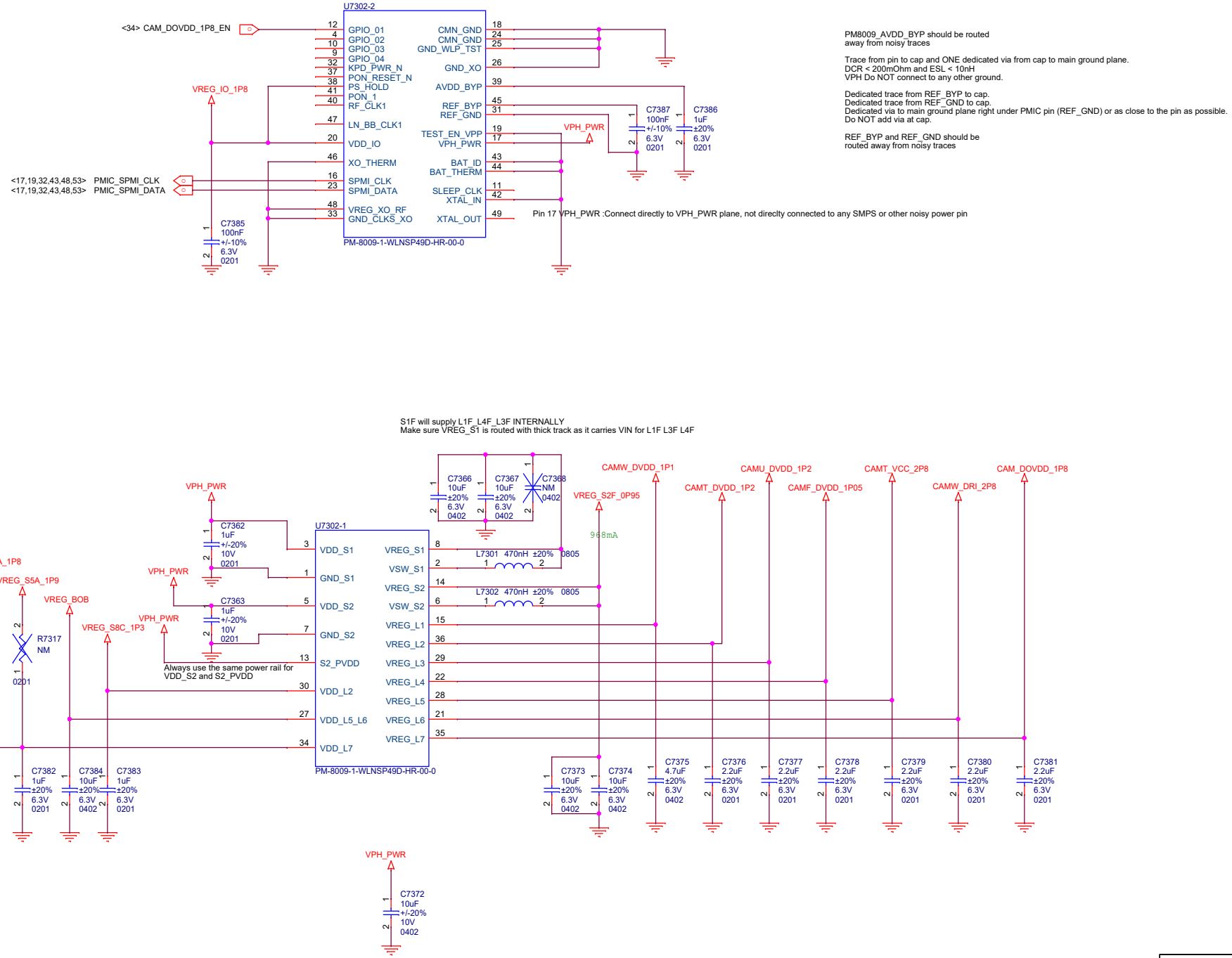

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